Single-IF DECT Receiver Architecture using a Quadrature Sub-sampling Band-pass Sigma-Delta Modulator

by

Simon A. Vieira-Ribeiro, B.A.Sc.

A
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submitted to the
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for the
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Ottawa-Carleton Institue for Electrical Engineering
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Department of Systems and Computer Engineering
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April, 1995

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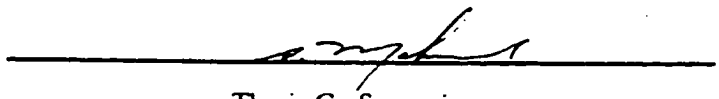

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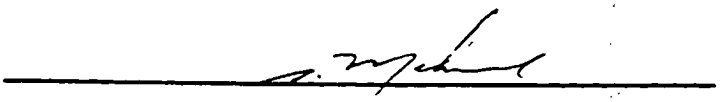

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ABSTRACT

The superheterodyne receiver architecture where there are multiple IF stages is still very common. This is because the multiple stages allows for increasing narrow-band filtering at each stage with the final goal of being able to select the desired RF channel (removing sufficiently adjacent channel, alternate channel and any other spurious interference). The mixing process at each stage also provides rejection as it mixes spurious that do not fall in the RF and IF frequency and image frequency bands away from the following stages. The cost to the receiver however is an increase in complexity. Thus there has been considerable research into the design of homodyne (zero-IF) and single-IF stage receivers as better filters become available.

A single-IF receiver architecture compliant to the DECT standard is described here. It takes advantage of the low-power transmission of this cordless system coupled with the TDMA scheme that is used as both these characteristics reduces the linearity requirements of the receiver and also reduces the maximum signal strength to be received by the receiver. This makes the filtering requirements of spurious interferers and the intermodulation products produced less stringent making it more suitable for a single-IF architecture with existing filter technology. The architecture also makes use of the high sampling rate of Sigma-Delta analog-digital converter to down convert the signal from the IF stage to base-band by applying quadrature sub-sampling techniques. The description includes an analysis of the overall system requirements, the system design of the receiver, the design and simulation of the band-pass Sigma-Delta analog-to-digital converter and the design of front-end radio frequency circuits.

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Simon Vieira-Ribeiro

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List of Abbreviations and Acronyms

ADC	Analog-to-Digital Converter
ADPCM	Adaptive Differential Pulse Code Modulation
AGC	Automatic Gain Control
AMPS	Advanced Mobile Phone Systems
AWGN	Additive White Gaussian Noise
BER	Bit-Error Rate
BiCMOS	Bipolar Complemetary Metal-Oxide-Silicon (fabrication process)
BPSDM	Band-pass Sigma-Delta Modulator
CDMA	Code-Division Multiple Access
CIR	Carrier to Interference Ratio
CMOS	Complementary Metal-Oxide-Silicon (fabrication process)
CPFSK	Continuous-Phase Frequency-Shift Keying
CRC	Cyclic Redundancy Check
CT1	Cordless Telecommunications 1
CT2	Cordless Telecommunications 2
CT2 Plus	Canadian Cordless Telecommunications 2
DCS	Dynamic Channel Selection
DDC	Direct-Down Conversion
DECT	Digital European Cordless Communications
DLC	Data Link Control
DQPSK	Differential Quadrature Phase Shift Keying
ECTEL	European Community Telecommunications
ETS	European Telecommunication Standard

ETSI	European Telecommunications Standards Institute
FDD	Frequency Division Duplex
FDMA	Frequency Division Multiple Access
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
FT	Fixed radio Termination (DECT)
FM	Frequency Modulation
FP	Fixed Part (DECT)
GHz	Gegahertz
GMSK	Gaussian Minimum Shift Keying
GSM	Groupe Special Mobile
I	In-phase component
IC	Integrated Circuits
IF	Intermediate Frequency
IIP3	Third Order Intercept Point referred to the input
IL	Insertion Loss
IMD	Intermodulation Distortion
IMR	Image Rejection Ratio
IS-54	North American Dual-Mode TDMA Cellular standard
LAN	Local Area Network
LNA	Low-Noise Amplifier
MAC	Medium Access Control
MHz	Megahertz
MOS	Metal-Oxide-Silicon
NF	Noise Figure

NMT	Nordic Mobile Telecom (Nordic cellular system at 400 MHz)
NRZ	Non-Return to Zero
NTP	Normal Transmitted Power
OIP3	Third Order Intercept Point referred to the output of the network
PBX	Private Business Exchange
PCS	Personal Communication Systems
P_{1dB}	1 dB compression point
PP	Portable Part (DECT)
PSK	Phase-Shift Keying
PT	Portable radio Termination DECT)
PTSN	Public Telephone Switching Network
Q	Quadrature component
QAM	Quadrature Amplitude Modulation
RFP	Radio Fixed Part (DECT)
RPE-LTP	Regular Pulse Excited Linear Prediction
RSSI	Received Signal Strength Indicator
SAW	Surface Acoustic Wave
sec	seconds
SNR	Signal-to-Noise Ratio
TACS	Total Access Communication System
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TOI	Third-Order Intercept
V	Volts
VSELP	Vector Sum Excited Linear Prediction

VSWR	Voltage Standing-Wave Ratio
$\pi/4$-QPSK	$\pi/4$-shift Quadrature Phase Shift Keying
$\Sigma\Delta$-ADC	Sigma-Delta Analog-to-Digital Converter

CHAPTER 1
INTRODUCTION

Wireless technology has recently become an area of great interest because of the introduction of second generation wireless portable telephones (digital wireless), personal digital assistants (Newton by Apple and EO 440 by AT&T) and the drive towards Personal Communication Systems (PCS). The second generation of wireless telecommunication standards that has been promoting the development of new wireless technologies, robust, power and cost effective architectures for use in the portable terminals are:

- Groupe Special Mobile (GSM): a pan-european digital cellular standard approved by the European Telecommunications Standards Institute (ETSI), introduced since 1989.
- IS-54: a North-American digital cellular standard that was to accommodate the use of both digital and analog systems in the same coverage area (dual-mode).
- CT2: a digital cordless telecommunications standard recently approved by ETSI but has been used in the United Kingdom and France for the past few years. It's Canadian equivalent is CT2 Plus.
- Digital European Cordless Telecommunications (DECT): also a European Telecommunication Standard (ETS) for digital cordless that was recently introduced in 1993.

The primary objective of this thesis will be to present a single-IF (intermediate frequency) digital receiver architecture that utilizes a band-pass Sigma-Delta Modulator (BPSDM) analog-to-digital converter to sub-sample the received signal at a high intermediate frequency (110 MHz) as a possible narrow-band wireless receiver architecture. The advantages of a single-IF architecture is to reduce the number of components required in

producing such wireless terminals which translate into lower cost in manufacturing such products as compared with the traditional dual-IF superheterodyne receiver structure. The advantages of using a BPSDM is that it allows both the control of the noise shaping function that attenuates quantization noise in the band of interest and the signal shaping function that will select the band of interest. Also the digitizing of the signal so early on in the receiver chain makes the structure more robust as it is less reliant upon analog signal processing.

The design of the receiver will adhere closely to the DECT standard. This standard was chosen because it is the most recently established of the four mentioned above and therefore will demonstrate quite sufficiently that the presented architecture is indeed applicable to modern portable wireless systems. It is also narrow-band and has constant envelope modulation (quite common in portable wireless systems including CT2 and GSM) both necessary requirements for this single-IF architecture.

This thesis will also present low-noise amplifier (LNA) and mixer circuits designed for use in the DECT standard. The objective of this was to design these circuits with their application in portable terminals in mind. Therefore they were designed to minimize their power consumption (used 3V power supplies) while still operating at 1.9 GHz (the carrier frequency for DECT). The intent of this was also to illustrate the effects and limitations of the chosen process technology on the design of the complete receiver system including the trade-offs between power consumption, noise and linearity.

1.1 Objective of the Thesis

The objective of this thesis is to design a single-IF receiver architecture that uses a band-pass sigma-delta modulator to sub-sample the IF GMSK signal and to convert that to its in-phase and quadrature components at baseband. The design of the receiver is to cover both the radio frequency front-end circuitry and the sigma-delta modulator.

1.2 Summary of Thesis Contribution

- Analysis of DECT requirements from the ETSI standard.
- Designing a sing e-IF receiver architecture that applies sub-sampling techniques to band-pass sigma-delta modulator that also incorporate quadrature demodulation in the process.
- Design and simulation of band-pass sigma-delta modulator including transfer function possible architecture and bit error-rate (BER) performance.
- Design simulation and fabrication of RF front-end circuitry and measurements from LNA. Performance specification to be used to demonstrate overall receiver performance.

1.3 Organization of Thesis

Chapter two starts off by describing the incentive to all the research into wireless systems, the marketing and sales success of cellular phones and cordless home-phones and the growing demand for these services. This is because the author feels that this is very relevant as it is the potential profitability of this product that drives the development and therefore research into these wireless products.The DECT standard is then presented with comparisons to other analog and digital standards. Particular attention is placed on the physical layer specifications.

Chapter three explain in detail the theories behind quadrature demodulation and how it is applied to the sub-sampling to reduce the amount of computations necessary to get the in-phase and quadrature components. Using these theories the single-IF architecture is developed and includes a gain, noise and linearity budget that includes specifications for the RF front-end circuitry and the analog-to-digital converter. The receiver requirements for direct conversion and single-IF conversion is compared.

Chapter four describes the theory and operation of Sigma-Delta Modulators using various examples. The design of the Band-pass Sigma-Delta Modulator is then presented including development of the Z-transfer functions that are optimized for noise performance. A possible architecture for implementation is also presented and simulations are performed to demonstrate the ability and stability of the modulator. Next, the decimator including its architecture is described and the combination of both modulator and decimator is simulated.

Chapter five presents the low-noise amplifier and mixer that were designed and fabricated for operations in the DECT frequency band and includes a description of the circuitry, its layout and simulations. The results from measurements made on the amplifier are also shown together with an illustration of the test apparatus and method that was critical to obtaining good reproducible results at these frequencies.

Chapter six concludes the thesis summarizing results and providing recommendations for further research.

CHAPTER 2

DIGITAL EUROPEAN CORDLESS TELECOMMUNICATION

2.1 INTRODUCTION

The cellular industry has been very successful with their introduction of the first generation of analog cellular equipment over the past decade. The number of subscribers has been increasing quite rapidly with many countries especially in Asia where the markets are still in their infancy. It has been estimated that the number of subscribers worldwide was at 23 million in January, 1993, increasing by 43% over the previous year (see fig. 2.1). The major growth areas were North America increasing by 46% (see fig 2.2), Australia by 54%, South Korea by 56% and China by 400% (with currently less than 50,000 users). With the average annual cost of using a cellular telephone to be about US$1536.79,where $512.26 were for fixed charges (annual rental and one third of the initial connection fee) and $1024.53 for airtime fees (total cost were averaged over many countries using calls of different distances at different times), the global revenues from providing cellular service would be about $35 billion alone. Another study [1] estimated the global market for cellular service at US$10 billion to $15 billion per year and also valued the sales of cellular equipment (network infrastructure and phones) to be $1 billion to $2 billion over the same time period. Thus it is obvious that the market for cellular products and services is very large and is continuing to grow quickly.

This increasing subscription put pressure on the system to increase its capacity, improve the security of the channel and to provide other wireless data services (faxes etc.) while maintaining the voice quality. Thus a new digital standard was developed for cellular communications resulting in the second generation of cellular standards (GSM, IS-54).

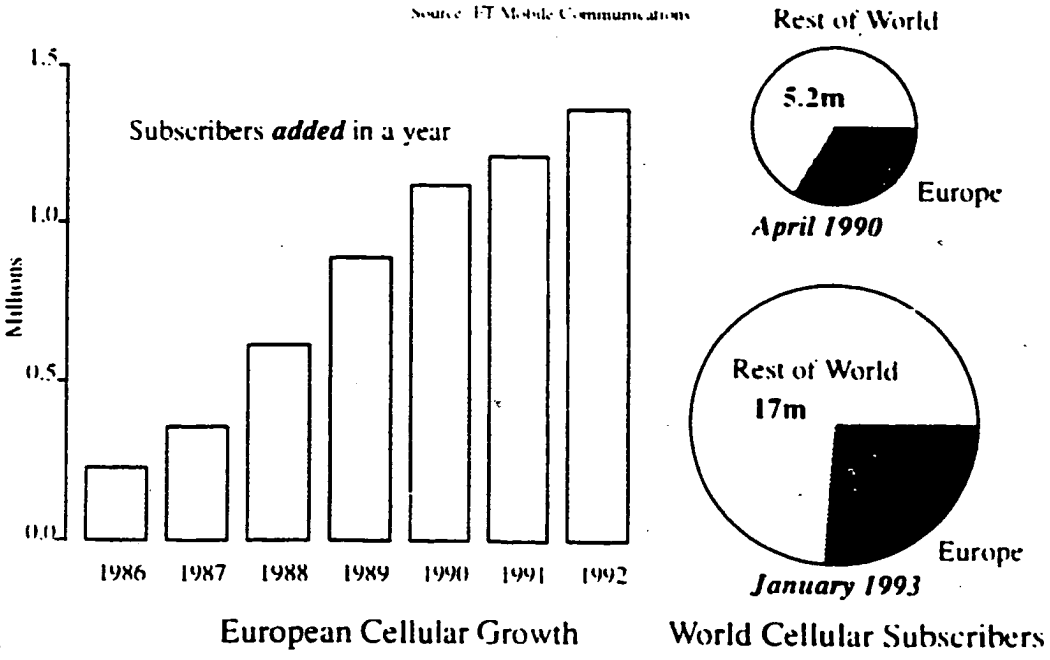


FIGURE 2.1 Cellular Growth of Europe compared to the Rest of the World

However even with these new systems, their capacity would still be insufficient for densely populated metropolitan cities unless a lot more spectrum is allocated (for example Hong Kong's cellular market is already quite saturated leading to increase in prices for subscription). Another growing market is the wireless private business exchanges (PBX) which would allow the office worker to be reached away from his/her desk and would perhaps, in the future, evolve to include wireless local-area networks (LANs) providing data services as well. Currently, the business office customer accounts for 60-80% of the revenues from telephone usage (the total market includes revenues from cellular systems, residential units etc.) and contains the highest density of users. It is envisioned that all these systems would ultimately merge to become a personal communication system (PCS) [2], "communications with anyone, anything, anywhere." All these applications require much greater capacity and greater data throughput than that capable with GSM and IS-54.

One method of increasing the capacity of current wireless systems is to decrease the size of the cells thus increasing the amount of frequency reuse. This is achieved by reducing the power of the transmitters in the base stations and the portable terminals effectively reducing the size of the cells. Another advantage of this is that the power consumption of the portable units will have decreased since less power would be required to communicate to the base stations that are now closer thus smaller batteries could be used [3] making the size of the units also smaller. It is with all these in mind that the digital cordless standards (CT2, DECT) were developed.

The purpose of this chapter is to introduce the DECT standard, particularly the physical layer requirements that the DECT receiver will be designed to meet in the later chapters. It starts by describing and comparing the existing common wireless standards and then begins to describe the DECT standard in slightly more detail with regards to the MAC layer processes (TDMA frame structure, Call set-up and handover, Dynamic Channel Selection) but covers in detail the Physical layer requirements as that applies directly to the radio re-

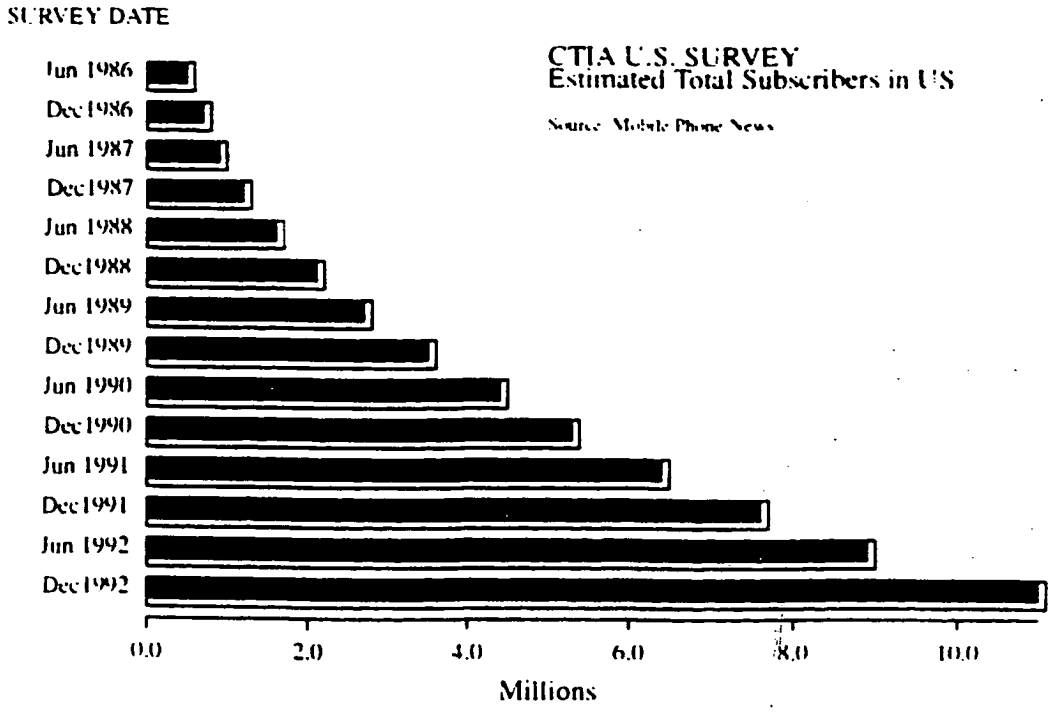


FIGURE 2.2 Cellular subscriber growth in the U.S.

ceiver. The overall RF system specifications that the DECT receiver must meet are then derived.

This chapter will use the same abbreviations as that used in the DECT standard (ETS 300 175)

2.2 DIGITAL WIRELESS STANDARDS

There are many different wireless standards currently in use around the world. The earlier (first generation) versions were "analog", that is they used analog frequency modulation (FM). Examples of these used to provide mobile cellular service include the Advanced Mobile Phone Systems (AMPS) used in countries including North America, Australia and New Zealand; the Total Access Communications System (TACS) which can be found in the United Kingdom, Ireland, Spain, Italy and Austria; and the Nordic Mobile Telecom (NMT) commonly found in scandinavian countries (Sweden, Norway, Denmark) and also including Finland, Switzerland, Luxembourg, Belgium, Netherlands, Iceland and Turkey. A common analog cordless standard was Cordless Telecommunications 1 (CT1) which operated in the 47 MHz frequency band.

The new second generation digital standards are now being introduced around the world. GSM is the pan-european cellular standard which originated in Europe but is now licensed in 34 countries including places as far away as Hong Kong and Singapore. IS-54 is a modification of AMPS to a digital system and is more of an interim solution (it appears that the North Americans are moving away from a single standard to possibly at least two digital standards with one using CDMA (Code-Division Multiple Access) and the other based on TDMA. CT2 (and its Canadian equivalent CT2 Plus [4]) is a cordless telecommunication standard that originated in the United Kingdom and its pan-european cousin is DECT. A brief summary of their system specifications can be found in table 2.1.

SYSTEM	AMPS	TACS	IS-54	GSM	CT2 Plus	DECT
Origin	N.America	UK	N.America	Europe	Canada	Europe
Modulation	Analog FM	Analog FM	DQPSK	GMSK	GMSK	GMSK
Freq [MHz] Allocation.	824-849 869-894	872-905 917-950	824-849 869-894	890-915 935-960	944-948	1881-1898
# of Carrier	832	1320	832	125	40,80	10
Transmit power [W]	0.6, 1.2, 3	0.6, 1.2, 3	0.6, 1.2, 3	2, 5, 8, 20	0.01	0.25
Multiple Access	N/A	N/A	TDMA	TDMA/ FDMA	FDMA	TDMA/ FDMA
Carrier spacing [kHz]	30	25	30	200	100	1728
Channels/ carrier	1	1	3, 6	8	1	10
Duplex	FDD	FDD	FDD	FDD	TDD	TDD
Channel Tx Rate [kb/s]	N/A	N/A	48.6	270.8	72	1152
Efficiency [b/s/Hz]	N/A	N/A	1.62	1.35	0.72	0.67
Voice Coding	N/A	N/A	VSELP 22.8 kb/s [8]	RPE-LTP 13 kb/s [9]	ADPCM 32 kb/s [10]	ADPCM 32 kb/s [10]

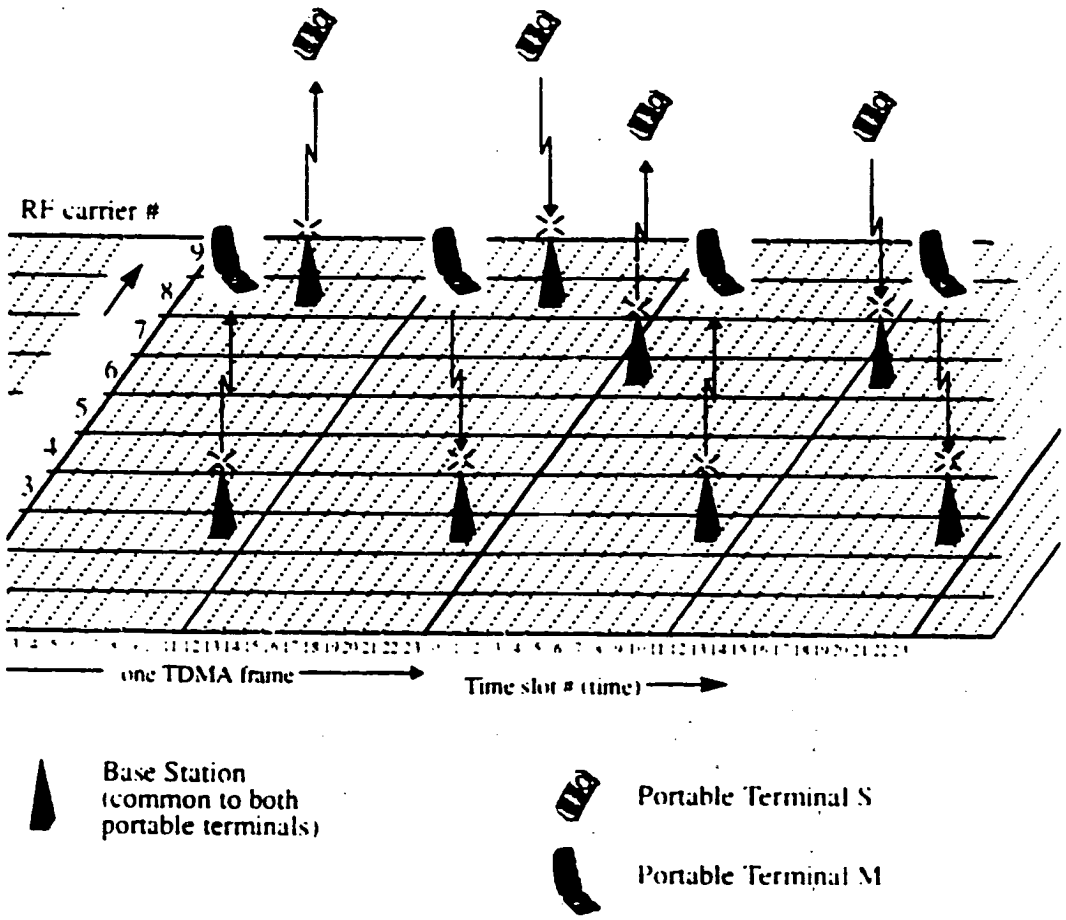
TABLE 2.1 Analog and Digital Wireless Standards

Although both cellular and cordless systems have a main common goal of providing access to the Public Telephone Switching Networks (PTSN), their intended customer and therefore application are quite different. The cellular systems are designed to service mobile user, these are users that move quite fast (i.e in a moving vehicle) thus their cells are quite large to avoid constant handovers between cells and also to provide coverage without too many cells. The large cell size however results in a lower capacity because of less frequency reuse per unit area. The complexity of the receiver is also increased because of the type of propagation characteristics that resulted from a moving transmitter/receiver with many physical obstacles in the transmission path (doppler spreading and multi-path fading and delay characteristics [8] requires antenna diversity and equalization in the receiver to counterbalance these effects).

Cordless systems were initially designed for the home where a cordless phone would only have to communicate with one base station. They have now evolved to being used in a more crowded environment like a large office complex where roaming from one cell to another is possible however the mobility of the user is still limited to a walking pace. The cells are smaller thus allowing for more frequency reuse (increasing the user capacity) and this in turn allows the terminals to be smaller as less power is needed to transmit between the base station and the portable terminal (also increases talk time). The propagation characteristics are also less disruptive thus equalization is not necessary (receiver architecture is simpler) and the transmission data rate can be higher (resulting in more users for voice service or higher data throughput for data services).

2.3 THE DECT STANDARD

The Digital European Cordless Telecommunication standard was produced by the ETSI Technical Committee, Radio Equipment and Systems, 3 (ETSI TC-RES3) in 1992 after consultation with many interest groups in the European Community (EC). It has therefore been allocated the necessary spectrum throughout the EC and is regulated by European



NOTE: physical channel for terminal M has not changed (same time slot, same carrier) but channel for terminal S has changed from carrier #8, slot 6 & 18 to carrier #6, slot 1 & 13. All performed by the same base station.

FIGURE 2.3 TDMA and FDMA in DECT

Law thus making DECT equipment compatible throughout Europe. The DECT standard evolved from the DCT-900, a Swedish Standard for Digital Cordless Telephones developed by Ericsson [19].

DECT uses both FDMA (10 carriers) and TDMA (12 duplex channels per carrier) to accommodate multiple users (see table 2.1). Thus the systems spaces its channels in two dimensions (frequency and time) allowing a link to be established with one user on carrier X in time slot N while another is in communication on carrier Y in time slot M and so on. A collision will occur only if both X = Y and N = M. CT2 uses FDMA where each different user must be assigned a unique carrier (1 channel per carrier). One of the main advantages of using TDMA is that it reduces the number of RF components in the base station (Fixed Part - FP) because one set of circuitry to receive and transmit the RF signal (one RFP) can establish upto 12 simultaneous (i.e in the same TDMA frame) duplex links in the 12 paired time slots (each pair contains an uplink and downlink time slot). Therefore DECT base stations will seldom need to contain more than one RFP whereas in CT2, the same number of RFPs are required for that number of simultaneous calls. However this is not Utopia and the trade off is that time synchronization of slots and frames is required. Another advantage is that the data transmission rate can easily be increased for a user by increasing the number of time slots per frame the user is allowed to communicate on, making it more flexible in providing data services. As long as the time slots are not the same, the data will still be transmitted in serial form thus the order of the data is easily preserved. In the limit where one user is allowed to use all the time slots per frame, the TDMA/FDMA DECT system becomes an FDMA system like CT2.

The following sections review briefly some important MAC layer processes, specifically the TDMA frame structure, handover, call setup, Dynamic Channel Selection (DCS). The physical layer specifications is covered in more details as it is relevant to defining the target performance of the receiver architecture in the next chapter. The reader is advised to

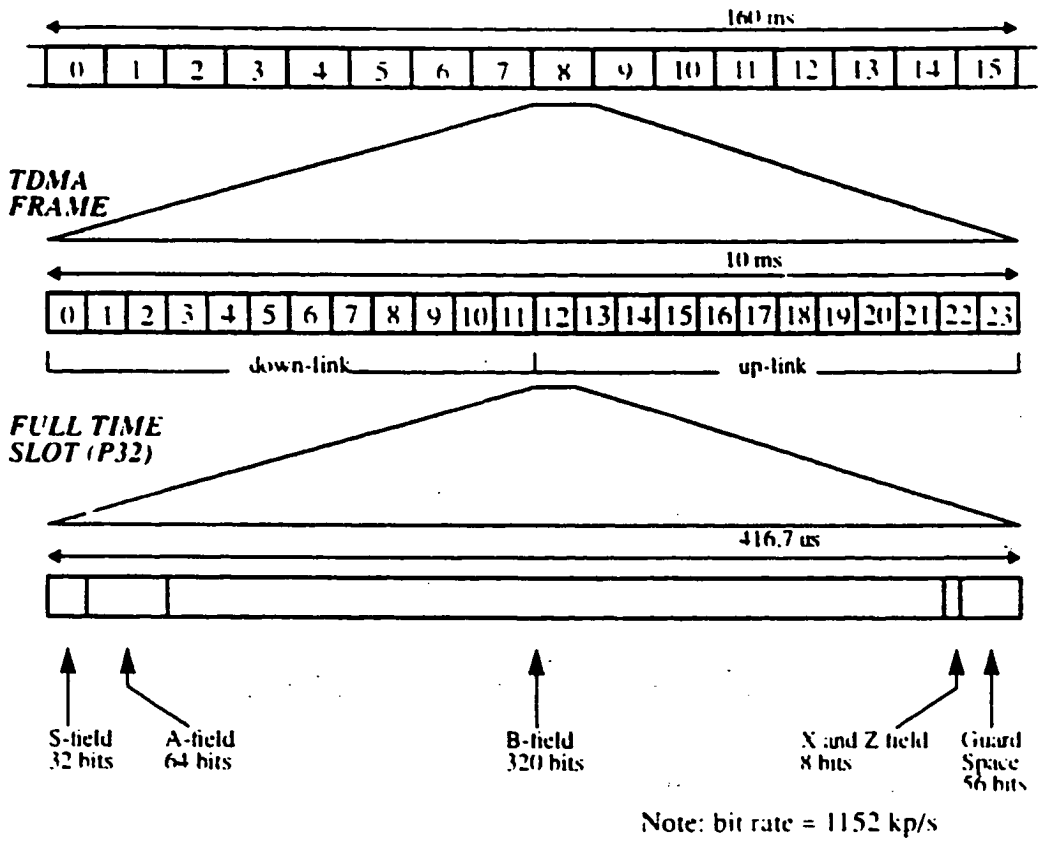


FIGURE 2.4 DECT TDMA frame structure

consult the actual ETSI documents [9], [10], [11], [12], [13], [14], [15], [16], [17] as final verification of the material presented

2.3.1 TDMA Frame Structure

The TDMA frame is 10 ms in duration and is divided into 24 time slots (numbered 0 to 23) of equal duration. The first 12 slots are used for down-links (base station to portable) and the remaining 12 are used for up links and are paired in the same order i.e slot 0 with slot 12 makes one duplex (TDD) pair 5 ms apart, slot 1 and slot 13 another etc.

Each time slot represents a full slot (P32) under normal 32 kb/s ADPCM voice or data transmission however two time slots can be combined to produce a double slot (P80) that can be used with ISDN terminals. The time slot can also be halved and is called a half slot (P08j). All of these slots consists of an S-field, a D-field that is made up of the A-field, B-field, X-field, and after the D-field follows the Z-field and a guard space (see section 4.4 of [10] and also see [11]).

- The S-field consists of a 16 bit preamble of alternating 1's and 0's for bit synchronization and a 16 bit sync word for slot synchronization.

  RFP S-field: 1010 1010 1010 1010 1110 1001 1000 1010 (binary)

  PF S-field: 0101 0101 0101 0101 0001 0110 0111 0101 (binary)

  (see section 4.6 in [10])

- The A-field is 64 bits long with a 48 bit control word and 16 bit CRC and is used to convey paging information, access rights identifiers and communication between software peers.

- The B-field varies in length depending on the slot type:

P32 (Full Slot)	320 bits of user data providing 32 kb/s in the 10 ms frame. If it is CRC protected (protected mode) then the 320 bits is divided into four 80 bit segments with 64 bits of data and 16 for CRC per segment (25.6 kb/s of data)

P80 (Double Slot)	800 bits of user data which gives 80 kb/s in unprotected mode and 64 kb/s in protected mode.
P08j (Half Slot)	80 bits long therefore has data throughput of 8 kb/s in unprotected mode and 6.4 kb/s in protected mode Subject to future standardization.

- X-field is a 4 bit redundancy check on the B-field (see [11])
- Z-field is a 4 bit repeat of the X-field for collision sensing (this is for early detection of an unsynchronized interference overlapping the end of the current packet P32, P08j, P80). See [11].
- Guard Space is 56 bits long.

2.3.2 Handset Synchronization

Each base station broadcast information continuously like a beacon on a dedicated "dummy" bearer and also on any other traffic bearer for handsets to listen to. This contains paging information (for call setup and requests), time slot and frame numbers for synchronization of the handset to the base station, the current systems capabilities (the services it can provide so that the handset does not request a service that can not be performed). The beacon (both dummy and traffic) can be identified from the A-field.

On entering a DECT system (i.e switching on or crossing into a new system) the handset will first synchronize to the "clearest" base station. This station is found by initially tuning into frequency 0, listening for the base station sync word for 10 ms, measuring and recording the signal strength of its transmission from the Received Signal Strength Indicator (RSSI) of the receiver, if something can be detected, and repeating for the other RF carriers. The chosen base station is that which has the highest RSSI and is used by the handset to synchronize with. Once synchronized calls can be established.

When there are no established calls, the handset is in sleep mode and awakes only once in every multi-frame (16 successive TDMA frames) to listen for any paging information. It will also resynchronize to the time slots at least once every 8 multi-frames.

2.3.3 Call Set-Up

Unlike CT2 the call set-up is controlled by the handset. A set-up can be initiated by the handset or it can be requested by the base station with a paging message. To set-up a bearer to the base station, a physical channel is chosen from a channel map that contains information on which are the clearest (this information is gathered from past monitoring of channels and stored by the handset) or perhaps from a suggested channels if the set-up request came from the base station. The channel map is not predetermined and channels are chosen according to the principles of Dynamic Channel Selection (DCS) as outlined in [18]. A bearer set-up request is then sent on the chosen channel (time slot and frequency) when the handset detects the base station is idle and listening in on that frequency (base station receiver scans all the RF carriers in a predetermined sequence). The base will then have half a TDMA frame to respond (i.e. on the down-link of the duplex bearer being established). Further details can be found in [11].

2.3.4 Bearer Handover Protocol

Handover is the process of changing communications from one physical channel to another. The handover can be within the cell (intra-cell handover) when for example the interference on the existing channel is deteriorating or the handover can be between different cells (inter-cell handover) to allow for roaming. The standard specifies a handover that is fast and seamless so as to maintain the quality of the communication channel (which can be greatly disrupted if the handover process is poor).

While a call is in progress, the handset will monitor the quality of the channel using the RSSI, CRCs from the A and B-fields, Z-field (for collision) and errors in the sync word in

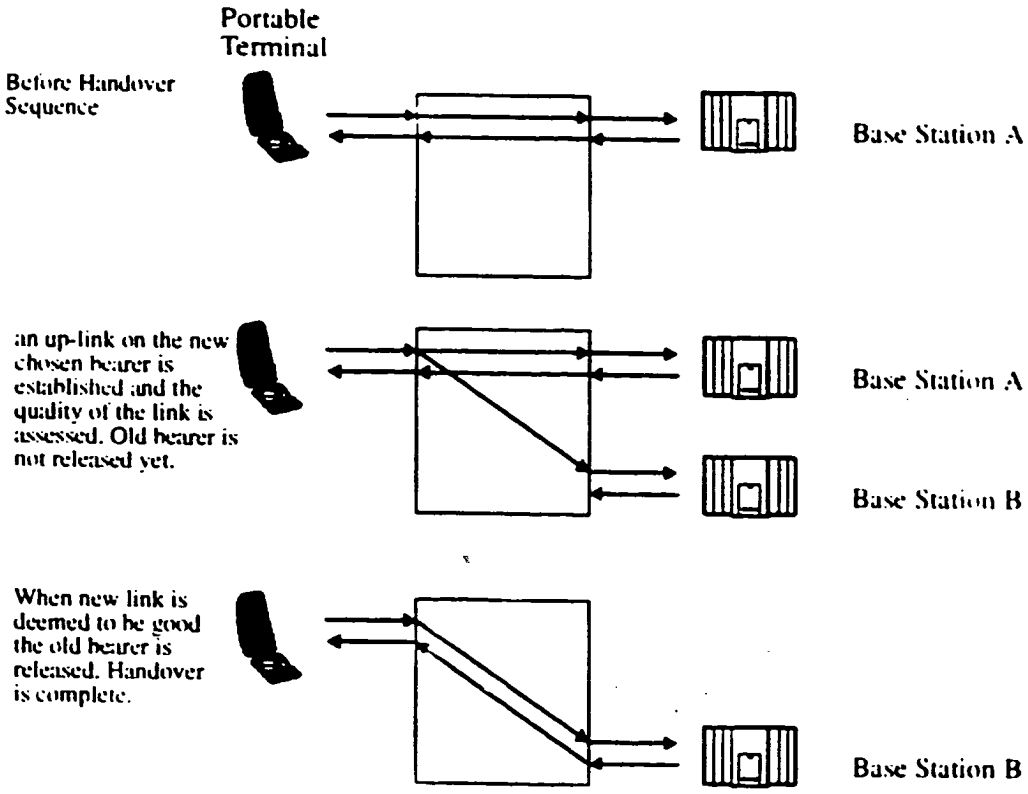


FIGURE 2.5 Handover Sequence in DECT

the S-field. If it is deemed unacceptable, the handset will initiate a handover. The base station can also monitor the quality of the link and report its findings to the handset but it is still upto the handset to initiate the handover. A new bearer is then selected from the channel map of the handset (if the best new channel is that which is from another base station then an inter-cell handover takes place) and a Bearer Handover Request is sent on the new time slot (cannot be the same as current bearer) when the base stations receiver's scan sequence reaches the chosen carrier. If no response (Bearer Confirm or Wait) is received in the corresponding down-link (in the time slot half a TDMA frame later) the process is aborted and repeated again (maximum of 15 attempts every 3 seconds so as to not increase the communication traffic). If the new duplex bearer is set-up successfully the old bearer is not immediately disconnected. Instead data is sent by the handset on both channels for at least one TDMA frame (and for a maximum of one multi-frame) and the data received by the base station from both channels are compared. The old bearer is released if the data received by the new bearer matches that of the old.

2.3.5 The Physical Layer

The Physical Layer primary function is the division of the frequency spectrum into it time, frequency and spatial dimensions. The MAC layer selects the physical channels and controls the connections on these channels but it is the physical layer that actually performs this task and is the interface between the MAC layer and the actual radio transmission medium.

The physical layer specifications for DECT can be found in [10] which separates them into 5 main parts:-

- Modulation and Demodulation of radio carriers of a certain channel bit rate to create a radio frequency channel.
- Synchronization of transmitters and receivers.

- Reception and Transmission of a specific number of data bits (packets) at a requested time and on a particular RF carrier.
- Addition and removal of S-field and Z-field.
- Measuring and recording RSSI.

Most of the information is rather self-explanatory and is therefore not reproduced here. However this section concentrates on calculating certain radio performance parameters e.g Third-Order Intercept (TOI) and Noise Figure (NF) for DECT receiver from the specifications in the physical layer. These parameters are more useful as they can be directly measured from the circuits as well as just being used to analyze the system performance of the receiver architecture in the next chapter.

2.3.5.1 Operating Temperature

Nominal temperature:	PP, FP, RFP, CCFP	+15 °C to +35 °C
Extreme temperature:	PP	0 °C to +40 °C
	FP, RFP, CCFP, class E1	+10 °C to +40 °C
	FP, RFP, CCFP, class E2	-10 °C to + 55 °C

Class E1 for installation in temperature controlled environments e.g. homes, offices etc.
Class E2 for all other installations
(see section 4 of [10])

2.3.5.2 RF carriers

The centre frequency (f_n) of each of the 10 RF carriers in DECT is given by:

$$f_n = f_0 - (1.728n) \text{ MHz}$$

where f_0 = 1897.344 MHz and n = 0,1.....9

The band of each RF carrier is from f_n - (1.728/2) MHz to f_n + (1.728/2) MHz and is designated RF channel n.

The transmitted carrier of an RFP on RF channel n must be within f_n 50 kHz under extreme conditions. For the PP, accuracy of 50 kHz relative to an absolute reference or relative to the received carrier is required under extreme conditions except when during the first 1 sec after transition from the idle-locked state to the active-locked state where the accuracy can be 100kHz relative to the received carrier (see section 4.1.1 and 4.1.2 of [10]).

2.3.5.3 Transmitted Power

For PPs and RFPs that have integral antennas (i.e. antenna permanently attached to RF circuitry), the equivalent isotropically radiated Normal Transmitted Power (NTP) shall be less than 250 mW for each simultaneously active transceiver under nominal conditions. If there is an external connector to the antenna (i.e. antenna can be disconnected), the NTP shall be less than 250 mW for each simultaneously active transceiver under extreme conditions when a matched load is connected to the antenna port. If there is more than one antenna port, the NTP is the sum of the instantaneous power from all the ports (see section 5.1, 5.2 and 5.3 of [10]).

2.3.5.4 RF Carrier Modulation

Modulation is Gaussian Frequency Shift Keying (GFSK), with a bandwidth-bit period (BT) product of nominally 0.5. GFSK is equivalent to GMSK.

A binary "1" is encoded with positive frequency deviation of +f where f = 288 kHz and therefore will have a peak transmit frequency of (f_n + f). A binary "0" results in a negative peak frequency deviation -f (see section 5.4 of [10]).

2.3.5.5 Receiver Sensitivity

The receiver sensitivity is defined as the power level at the receiver input such that the Bit-Error Rate (BER) in the D-field is 0.001 and shall be -83 dBm. The maximum signal to be received at the receiver is -14 dBm. The Noise Figure of the receiver system (see Appendix B) can computed knowing the sensitivity limit of the receiver. Using the fact that the Signal-to-Noise Ratio per bit (γ_b) required to demodulate a GMSK signal non-coherently is 13.6 dB [37] equation (B19) of Appendix B can be rewritten as

$$NF = P_{min} - 10 \cdot \log(\gamma_b) - 10 \cdot \log(R_b) + 174. \qquad \text{(EQ 2.1)}$$

Now for DECT, $R_b = 1.152\ (10^6)$ bits/s and $P_{min} = -83$ dBm therefore the NF is

$$NF = -83 - 13.6 - 10 \cdot \log(1.152 \cdot 10^6) + 174 = 16.8$$

(see 6.2 and 6.5.2 of [10]).

2.3.5.6 In-band Interference

The receiver must be able to demodulate data successfully (BER of less than 0.001 for the D-field) when the desired RF channel M's signal strength is -73 dBm while another single DECT interferer is active in another RF channel Y with signal strength for the different values of Y given in table 2.2.

Thus the co-channel Carrier to Interference Ratio (CIR) can be deduced from Y = M interferer to be 10 dB (-73 + 83) when the desired channels signal strength is -73 dBm. Also the Adjacent channel CIR is -73 + 58 = -15 dB (see section 6.4 of [10]).

2.3.5.7 Out-of-Band Interference

The receiver must be able to demodulate data with a BER of less than 0.001 in the D-field when the desired signal in the DECT band is at -80 dBm (carrier frequency f_c) while sub-

Interferer on RF channel Y	Interferer signal strength [dBm]	Comments
Y = M	-83	Co-channel interference
Y = M 1	-58	Adjacent-channel interference
Y = M 2	-39	
Y = any other DECT channel	-33	

TABLE 2.2 In-band interference specification

Interferer Frequency (f)[MHz]	Interferer signal strength [dBm]
$25 \le f < 1780$	-23
$1780 \le f < 1875$	-43
$\lvert f - f_c \rvert > 6$	-43
$1905 \le f < 2000$	-43
$2000 \le f < 12750$	-23

TABLE 2.3 Out-of-band Interference specifications

ject to a single interferer (which may be a modulated carrier or single frequency tone) in any of the frequency bands with the corresponding power levels given in table 2.3 (see section 6.5.1 and 6.1.1 of [10]).

2.3.5.8 Intermodulation and Linearity

Amplifier are inherently non-linear and when required to amplify two tones, the amplifier not only produces two amplified tones at their corresponding frequencies but also produces other tones (see Appendix B). This intermodulation distortion has its largest component adjacent on either side of the two desired tones offset in frequency by the same separation between the 2 desired tones. These 2 distorting components are called the Third-Order Intermodulation Products.

TDMA inherently relaxes the intermodulation requirements of the system because in order for intermodulation distortion (IMD) to affect a certain RF channel (channel number M), there must be other interferers in the adjacent RF channels (channel numbers X and Y) such that X and Y are both greater than or both less than M and they must all be equally spaced apart in frequency. Also in order for interference to occur they must also be transmitting in the same time slot. Since in most applications a basestation will need only one REP then intermodulation distortion is unlikely to occur (requires 3 REPs from either the same basestation or from different basestations closeby so that simultaneous transmissions on the same RF channel is possible). However because DECT is required to work in a hostile environment where there maybe another DECT system present or closeby then a reasonable amount of linearity is prudent.

The receiver must be able to demodulate a signal of strength -80 dBm with a BER of less than 0.001 while subject to interference from two DECT interferers in different RF carriers such that their intermodulation product is on the same RF carrier as the desired signal.

The signal strength of the interferers is -46 dBm (-80dBm + 34 dB). Neither of the two interferers can be adjacent to the desired channel.

The TOI (see Appendix B) at the input to the receiver can be computed from these values and results in 2 different numbers depending upon which assumptions are made. If the CIR of 10 dB for a co-channel interferer is used (see previous section), the intermodulation product created by the 2 interfering signals must be 10 dB below the signal in the desired channel the input third order intercept point (IIP3)is given by equation (B27) of Appendix B

$$IIP3 = -46 + \frac{(-46 - (-80 - 10))}{2} = -24 \text{ dBm.} \qquad \text{(EQ 2.2)}$$

If instead, the interference level of the desired channel is to be no greater than the acceptable noise for non-coherent demodulation of GMSK then the SNR per bit (γ_b) must be used and the noise level must be at least the NF below the signal level (see section 2.3.5.5 and Appendix B) i.e. x_3 in (B27) = -80 - NF = -80 - 16.8 = -96.8. Thus the intercept point is

$$IIP3 = -46 + \frac{(-46 - (-80 - 16.8))}{2} = -20.6 \text{ dBm.}$$

2.3.5.9 Other Issues

Since in each FT in a base station any of the 10 RF carriers may be used, the synthesizer in the FT must be able to transverse the whole DECT bandwidth (all the carriers) within the guard time of 56 bits (approx. 50 µs) and this must include the settling time after the synthesizer has switched frequencies. This requirement is less stringent at the PT of the portable terminal as communication is done every TDMA frame.

Also the power ramp-up and ramp-down times during transmission transitions must also be accurately controlled. These and many other issues have not been presented here as they are not relevant to this thesis and further details can be found in [10].

2.4 Conclusion

The DECT standard uses GMSK modulation at a data rate of 1.152 Mbps at transmission/reception (TDD) frequencies in the DECT RF band of 1881-1898 MHz which spans the 10 RF channels equally spaced by 1.728 MHz. The radio's sensitivity is rather modest in comparison to cellular radio standard due to the difference in cell sizes and the TDMA/FDMA scheme has been shown to reduce the intermodulation requirements. Both these factors will be demonstrated in chapter 4 to be advantageous towards the use of the single-IF architecture described in chapter 3.

The following parameters derived in previous sections are necessary in order for a radio receiver to be compliant with the DECT standard:

- Sensitivity = -83 dBm
- Maximum signal strength = -14 dBm
- Noise Figure = 16.8 dB
- Input Third Order Intercept = -20.6 dBm
- Co-channel CIR = 10 dB

Note: These power levels are all referred to the input of the receiver.

These specifications will be used in the following chapters to determine the radio architecture and to define the various parameters the components of the receiver must have such that the overall system would be compliant.

CHAPTER 3

DIGITAL RECEIVER ARCHITECTURE AND SYSTEM REQUIREMENTS

3.1 INTRODUCTION

The role of the receiver is to recover the information sent by the corresponding transmitter. This almost always involves the amplification of the incident signal so that the receiver can detect (demodulate) signals with low power levels (a receiver's sensitivity is a measure of its ability to detect very weak signals - see appendix B). The receiver must also be able to distinguish the desired signal from other signals of neighbouring frequencies (its selectivity) and this is achieved by filtering. All the digital wireless receivers currently being used in practice perform these tasks but they use different architectures because of the wide variety of wireless applications in existence. Their relative performances differ depending upon the intended usage because of the trade off for certain more important (application specific) system parameters at the expense of other less crucial ones (the engineering dilemma). However they are all designed to attain good sensitivity, selectivity and dynamic range (the power range of the input signal that can be processed by the receiver).

Modern architectures date back to the superheterodyne principle proposed by E.H. Armstrong [20] which was to fix the frequency response of the amplifiers and filters and shift the input signal frequency to be within their operating range as opposed to the earlier techniques of using tunable amplifiers and mixers and moving their frequency band to cover the input signal. This was an improvement because the fixed-frequency response components performed better than their tunable counterparts. This principle is still used in the current architectures but most have two IF stages as in figure 3.1

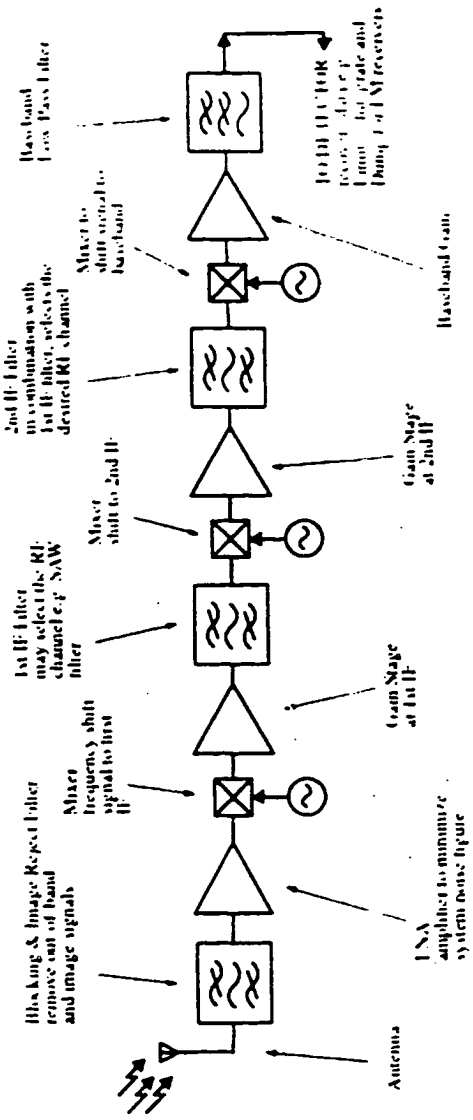


FIGURE 3.1 Superheterodyne receiver architecture

Recently advances in both semiconductor technology and analog-to-digital converters have allowed system designers to develop receiver architectures that reduce the number of IF stages and to demodulate the signal digitally using digital signal processes. The motivation behind reducing the number of IF stages is to reduce the number of components (mixers, oscillators and filters) necessary and therefore reduce the cost to manufacture those receivers (there maybe some power savings too). The advantage to demodulating digitally is that the signal processing is reproducible, predictable and can be changed without altering the hardware. There is also greater reliability with temperature and time.

This chapter discusses two architectures that are receiving currently the most attention as possible alternatives to the conventional multi-IF stage superheterodyne systems. They are the Direct-Down Conversion (or Zero-IF) receiver and the Single-IF receiver. Both these architectures involve digital quadrature demodulation and so this is covered first. The Direct-Down Conversion receiver is then described and is shown to be not a good solution particularly due to low-frequency pick-up. The Single-IF receiver is demonstrated to be a good compromise between the conventional superheterodyne and direct-down conversion methods.

Now that the basic architecture has been determined, the basic system requirements of each block are then derived such that the receiver will meet the DECT sensitivity and intermodulation specifications.

3.2 DIGITAL QUADRATURE DEMODULATION

Quadrature demodulation of a signal involves resolving this signal into its in-phase (I) and quadrature components (Q) at baseband. The I and Q components can then be used to extract the data information for most common narrowband modulation schemes (e.g. M-ary PSK, QAM, CPFSK).

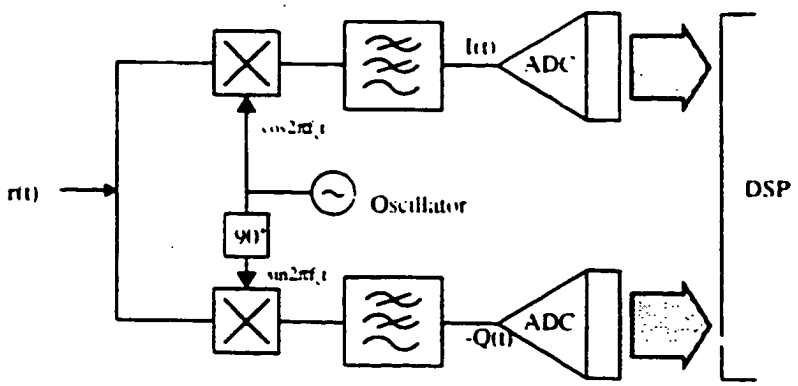


FIGURE 3.2 Digital Quadrature Demodulation

3.2.1 The Principle

This narrow band signal received at the antenna and centred at the RF carrier frequency f_c can be ideally represented by

$$r(t) = A(t) \cdot \cos(2\pi f_c t + \varphi(t)) \qquad \text{(EQ 3.1)}$$

where A(t) is the time-varying amplitude (envelope) of r(t) and φ(t) is the time-varying phase. Equation (3.1) can be further expanded to reveal the I and Q components

$$r(t) = A(t) \cdot (\cos(\varphi(t)) \cos 2\pi f_c t - \sin(\varphi(t)) \sin 2\pi f_c t). \qquad \text{(EQ 3.2)}$$

The in-phase component is

$$I(t) = A(t) \cdot \cos(\varphi(t)) \qquad \text{(EQ 3.3a)}$$

and the quadrature component is

$$Q(t) = A(t) \cdot \sin(\varphi(t)). \qquad \text{(EQ 3.3b)}$$

To extract these baseband components (independent of the carrier frequency), the received signal r(t) is first multiplied with a sinusoidal wave that is either in-phase or quadrature to the RF carrier

$$\begin{aligned} r(t) \cos 2\pi f_c t = {} & \frac{A(t)}{2} \cdot \cos(\varphi(t)) \\ & + \frac{A(t)}{2} \cdot \cos(\varphi(t)) \cos(4\pi f_c t) \\ & - \frac{A(t)}{2} \cdot \sin(\varphi(t)) \sin(4\pi f_c t) \end{aligned} \qquad \text{(EQ 3.4a)}$$

$$\begin{aligned} r(t) \sin 2\pi f_c t = {} & -\frac{A(t)}{2} \cdot \sin(\varphi(t)) \\ & + \frac{A(t)}{2} \cdot \sin(\varphi(t)) \cos(4\pi f_c t) \\ & + \frac{A(t)}{2} \cdot \cos(\varphi(t)) \sin(4\pi f_c t) \end{aligned} \qquad \text{(EQ 3.4b)}$$

and then low-pass filtered to remove the high frequency terms.

Thus the instantaneous phase $\varphi(t)$ can be computed from I and Q

$$\varphi(t) = \text{atan}\left(\frac{Q(t)}{I(t)}\right) \qquad \text{(EQ 3.5)}$$

and the magnitude A(t) is given by

$$A(t) = \sqrt{(I(t))^2 + (Q(t))^2}. \qquad \text{(EQ 3.6)}$$

In practice the I and Q components are sampled and converted to a digital representation thus the magnitude and phase can be computed digitally or obtained through a look-up table.

It is worth noting here that in certain modulation schemes in which the envelope is constant with time (e.g. GMSK), all the information can be recovered from just the phase (A(t) does not vary with the data symbols and therefore it is not necessary to recover the amplitude A(t) therefore limiters can be used in the receiver architecture. However in some cases where the signal gain in the receiver is variable, some measure of the amplitude of the signal is required as part of the gain control. Another common wireless modulation scheme that does not require the amplitude information (i.e can use a limiter) is $\pi/4$-QPSK (used in IS-54) [21].

3.2.2 The Effects of Gain and Phase Mismatch in Quadrature Demodulation

In the previous section, it was assumed that there are no gain or phase mismatches between the in-phase and quadrature branches. This is of course is not necessarily the case. These non-idealities occur in practical realizations of the mixers, amplifier, filters and the 90 degrees phase shifter. The effects of phase mismatch can be derived from the following:

Let $r(t) = A\cos(2\pi f_c t + \varphi)$ and account for the gain and phase mismatch by assuming that the gain in the in-phase branch is off by a factor of α (normally $\alpha = 1$) and the phase error offset by φ_e (normally $\varphi_e = 0$). Also assume that the oscillator frequency is f_0. Thus the output of the mixer in the I branch is

$$I_{mix}(t) = r(t) \cdot \alpha\cos(2\pi f_o t - \varphi_e) \qquad \text{(EQ 3.7)}$$

and low-pass filtered this becomes

$$\begin{aligned} I(t) &= \alpha \cdot A\cos(2\pi (f_c - f_o) t + \varphi_e + \varphi) \\ &= \alpha \cdot A\cos(2\pi f_{IF} t + \varphi_e + \varphi). \end{aligned} \qquad \text{(EQ 3.8)}$$

The output of the mixer in the Q branch is

$$Q_{mix}(t) = r(t) \cdot \sin 2\pi f_o t. \qquad \text{(EQ 3.9)}$$

After filtering it becomes

$$\begin{aligned} Q(t) &= A\sin(2\pi (f_c - f_o) t + \varphi) \\ &= A\sin(2\pi f_{IF} t + \varphi). \end{aligned} \qquad \text{(EQ 3.10)}$$

Now let $u(t) = I(t) + jQ(t)$, the complex envelope of the signal after being corrupted with the mismatches in the branches

$$\begin{aligned} u(t) &= \alpha \cdot A\cos(2\pi f_{IF} t + \varphi_e + \varphi) + j(A\sin(2\pi f_{IF} t + \varphi)) \\ &= \frac{A}{2} \cdot [e^{j\varphi}(\alpha e^{j\varphi_e} + 1) e^{j2\pi f_{IF} t} + e^{-j\varphi}(\alpha e^{-j\varphi_e} - 1) e^{-j2\pi f_{IF} t}]. \end{aligned} \qquad \text{(EQ 3.11)}$$

The Fourier Transform of $u(t)$ is

$$U(f) = \frac{A}{2} \cdot [e^{j\varphi}(\alpha e^{j\varphi_e} + 1)\delta(f - f_{IF}) + e^{-j\varphi}(\alpha e^{-j\varphi_e} - 1)\delta(f + f_{IF})]. \qquad \text{(EQ 3.12)}$$

Now the real signal spectrum of this complex envelope is given by

$$S(f) = \frac{U(f) + U^*(-f)}{2}. \qquad \text{(EQ 3.13)}$$

Therefore

$$\begin{aligned} S(f) &= \frac{A}{4} \cdot \left[e^{j\varphi} (\alpha\cos\varphi_e + 1 + j\alpha\sin\varphi_e)\, \delta(f - f_{IF}) \right] \\ &+ \frac{A}{4} \cdot \left[e^{-j\varphi} (\alpha\cos\varphi_e - 1 - j\alpha\sin\varphi_e)\, \delta(f + f_{IF}) \right] \\ &+ \frac{A}{4} \cdot \left[e^{-j\varphi} (\alpha\cos\varphi_e + 1 - j\alpha\sin\varphi_e)\, \delta(-f - f_{IF}) \right] \\ &+ \frac{A}{4} \cdot \left[e^{j\varphi} (\alpha\cos\varphi_e - 1 + j\alpha\sin\varphi_e)\, \delta(-f + f_{IF}) \right] \end{aligned} \qquad \text{(EQ 3.14)}$$

$$\begin{aligned} \therefore \quad S(f) &= \frac{A}{4} \cdot \left[e^{j\varphi} (\alpha\cos\varphi_e + 1 + j\alpha\sin\varphi_e) \right. \\ &\qquad \left. + e^{j\varphi} (\alpha\cos\varphi_e - 1 + j\alpha\sin\varphi_e) \right] \delta(f - f_{IF}) \\ &+ \frac{A}{4} \cdot \left[e^{-j\varphi} (\alpha\cos\varphi_e - 1 - j\alpha\sin\varphi_e) \right. \\ &\qquad \left. + e^{-j\varphi} (\alpha\cos\varphi_e + 1 - j\alpha\sin\varphi_e) \right] \delta(f + f_{IF}). \end{aligned}$$

This is obviously consistent with the Fourier Transform of the real part of u(t) however it can be rewritten as the spectrum of 2 cosine waves of different magnitudes

$$\begin{aligned} S(f) &= \frac{A}{4} \cdot \left[e^{j\varphi} (\alpha\cos\varphi_e + 1 + j\alpha\sin\varphi_e)\, \delta(f - f_{IF}) \right. \\ &\qquad \left. + e^{-j\varphi} (\alpha\cos\varphi_e + 1 - j\alpha\sin\varphi_e)\, \delta(f + f_{IF}) \right] \\ &+ \frac{A}{4} \cdot \left[e^{j\varphi} (\alpha\cos\varphi_e - 1 + j\alpha\sin\varphi_e)\, \delta(f - f_{IF}) \right. \\ &\qquad \left. + e^{-j\varphi} (\alpha\cos\varphi_e - 1 - j\alpha\sin\varphi_e)\, \delta(f + f_{IF}) \right]. \end{aligned} \qquad \text{(EQ 3.15)}$$

Notice that for the ideal case where $\alpha = 1$ and $\varphi_e = 0$, the former cosine term is in-phase and the latter cosine term disappears. Thus the former term can be considered the desired

tone and the latter can be thought of as an image mixed down to the IF frequency when there are no mismatches in the process

Therefore the IQ mismatch can be expressed in terms the image rejection ratio (IMR) where ideally the image is totally rejected.

$$IMR = \frac{(\alpha\cos\varphi_e - 1)^2 + (\alpha\sin\varphi_e)^2}{(\alpha\cos\varphi_e + 1)^2 + (\alpha\sin\varphi_e)^2} = \frac{\alpha^2 + 1 - 2\cdot\cos\varphi_e}{\alpha^2 + 1 + 2\cdot\cos\varphi_e}. \qquad \text{(EQ 3.16)}$$

It is from this equation that one can calculate one degree in phase error ($\varphi_e = 1^\circ$) results in an image rejection (or protection) of about 40 dB. This is often stated in many papers ([22], [23],[24],[25]) without elaboration.

Another obvious effect of IQ mismatch is that the BER deteriorates due to the errors in the detected signal constellation. If the mismatch is not relatively constant then it can not be accounted for in the receiver and has a net effect of increasing the variance of the signal from its ideal position in the constellation resulting in the BER increasing.

3.2.3 Quadrature Sampling

One method of eliminating the gain and phase mismatches between the in-phase and quadrature paths is by sampling the signal at four times its carrier (or IF) frequency and down converting the sampled signal down to baseband digitally to obtain the I and Q components (assume there is no aliasing because the signal bandwidth is much smaller than the carrier frequency - narrowband signal).

Recall from equation (3.2) that

$$r(t) = I(t)\cos 2\pi f_c t - Q(t)\sin 2\pi f_c t. \qquad \text{(EQ 3.17)}$$

The Fourier Transform gives

$$R(f) = I(f) \otimes \left(\frac{1}{2}\delta(f-f_c) + \frac{1}{2}\delta(f+f_c)\right) - Q(f) \otimes \left(\frac{1}{2j}\delta(f-f_c) - \frac{1}{2j}\delta(f+f_c)\right) \quad \text{(EQ 3.18)}$$

where I(f) is the Fourier Transform of i(t) and similarly for Q(f).

The sampled signal spectrum of r(t) becomes (f_s = sampling frequency)

$$R_s(f) = I(f) \otimes \frac{1}{T_s}\sum_{n=-\infty}^{\infty}\left(\frac{1}{2}\delta(f-f_c-nf_s) + \frac{1}{2}\delta(f+f_c-nf_s)\right) - Q(f) \otimes \frac{1}{T_s}\sum_{n=-\infty}^{\infty}\left(\frac{1}{2j}\delta(f-f_c-nf_s) - \frac{1}{2j}\delta(f+f_c-nf_s)\right). \quad \text{(EQ 3.19)}$$

To obtain the baseband in-phase component I(f) from the sampled signal $r_s(t)$, as in the continuous time domain, $r_s(t)$ is multiplied with $\cos 2\pi f_c t$

$$r_s(t) = \sum_{n=-\infty}^{\infty} r(nT_s)\cdot\delta(t-nT_s)$$

$$\therefore \quad r_s(t)\cos 2\pi f_c t = \sum_{n=-\infty}^{\infty} r(nT_s)\cos(2\pi f_c nT_s)\cdot\delta(t-nT_s). \quad \text{(EQ 3.20)}$$

And the Fourier Transform of this is

$$\begin{aligned} FT\{r_s(t)\cos 2\pi f_c t\} &= R_s(f) \otimes \left(\frac{1}{2}\delta(f-f_c) + \frac{1}{2}\delta(f+f_c)\right) \\ &= I(f) \otimes \frac{1}{4T_s}\sum_{n=-\infty}^{\infty}\left(\delta(f-2f_c-nf_s) + \delta(f-nf_s)\right. \\ &\qquad \left. + \delta(f-nf_s) + \delta(f+2f_c-nf_s)\right) \quad \text{(EQ 3.21a)} \\ &\quad - Q(f) \otimes \frac{1}{4T_s j}\sum_{n=-\infty}^{\infty}\left(\delta(f-2f_c-nf_s) - \delta(f-nf_s)\right. \\ &\qquad \left. - \delta(f-nf_s) - \delta(f+2f_c-nf_s)\right) \end{aligned}$$

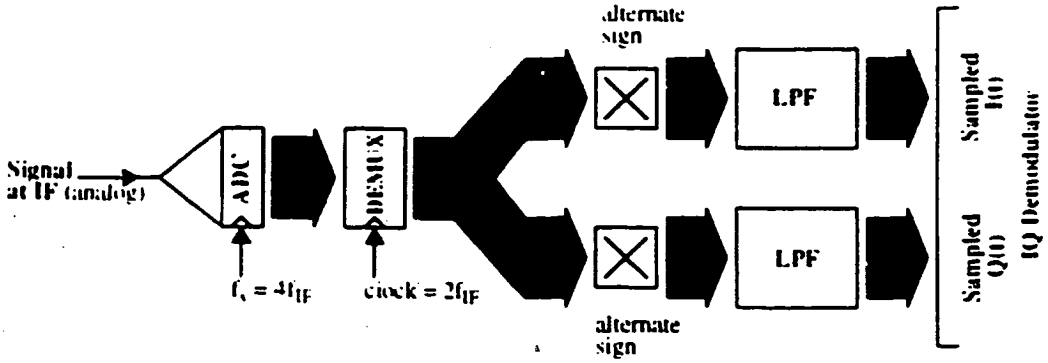


FIGURE 3.3 Quadrature Sampling

$$= I(f) \odot \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \left(\frac{1}{2}\delta(f - nf_s) + \frac{1}{4}\delta(f - 2f_c - nf_s) + \frac{1}{4}\delta(f + 2f_c - nf_s) \right)$$

$$-Q(f) \odot \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \left(\frac{1}{4j}\delta(f - 2f_c - nf_s) - \frac{1}{4j}\delta(f + 2f_c - nf_s) \right) \qquad \text{(EQ 3.21a)}$$

$$= \left(\frac{1}{2}I(f) + \frac{1}{4}I(f - 2f_c) + \frac{1}{4}I(f + 2f_c) \right) \odot \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - nf_s)$$

$$- \left(\frac{1}{4j}Q(f - 2f_c) - \frac{1}{4j}Q(f + 2f_c) \right) \odot \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - nf_s).$$

The final expression in equation (3.21a) shows clearly how the signal is replicated and it can be deduced that there will be a replica of I(f) at the baseband when the index n = 0. All the higher frequency components have to be digitally filtered.

A similar analysis can be done to show how to obtain the baseband component Q(f) from $r_s(t)$

$$\text{FT}\{r_s(t) \sin 2\pi f_c t\} =$$

$$\left(\frac{1}{4j}I(f - 2f_c) - \frac{1}{4j}I(f + 2f_c) \right) \odot \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - nf_s)$$

$$+ \left(-\frac{1}{2}Q(f) + \frac{1}{4}Q(f - 2f_c) + \frac{1}{4}Q(f + 2f_c) \right) \odot \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - nf_s).$$

Note that there has been no condition placed on the relationship between f_s and f_c in deriving these equations so far however the need for $f_s = 4f_c$ comes from equation (3.20). However, from (3.21a) and (3.21b) it can be deduced that elimination of aliasing requires that the $f_c > 2BW$ and that $f_s > 2f_c + BW$ where BW is the baseband bandwidth of the desired signal.

Using this relationship between the sampling frequency and centre frequency of the signal the multiplication of $r_s(t)$ with $\cos 2\pi f_c n T_s$ and $\sin 2\pi f_c n T_s$ in the sampled domain becomes a trivial multiplication with {1, 0, -1, 0, 1, ...} for the cosine and {0, 1, 0, -1, 0, ...} for the sine. Thus every other sample of $r_s(t)$ belongs to the I branch (with alternating sign) and the other samples belong to the Q branch. This also simplifies the hardware (see figure 3.3)

3.2.4 Quadrature Sub-sampling

In the previous section, $f_s = 4f_c$ was found to be a very convenient for implementation which also does not cause any aliasing with the baseband I/Q component. Fortunately this is a subset of the frequencies which also yield this advantage.

The reason that $f_s = 4f_c$ was chosen was because $\cos 2\pi f_c n T_s$ becomes the sequence {1, 0, -1, 0, 1, ...} which makes multiplication with $r_s(t)$ in equation (3.20) very simple therefore this condition is retained. However the assumption that the centre frequency of the signal r(t) is equal to f_c can be removed. Rewrite equation (3.17) with the centre frequency = f_{IF}

$$r(t) = I(t)\cos 2\pi f_{IF} t - Q(t)\sin 2\pi f_{IF} t \qquad \text{(EQ 3.22)}$$

equation (3.19) becomes

$$\begin{aligned} R_s(f) = I(f) \otimes \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \left(\frac{1}{2}\delta(f - f_{IF} - nf_s) + \frac{1}{2}\delta(f + f_{IF} - nf_s) \right) \\ - Q(f) \otimes \frac{1}{T_s} \sum_{n=-\infty}^{\infty} \left(\frac{1}{2j}\delta(f - f_{IF} - nf_s) - \frac{1}{2j}\delta(f + f_{IF} - nf_s) \right). \end{aligned} \qquad \text{(EQ 3.23)}$$

Applying this to the analysis in the previous section finally results in a more general version of equation (3.21a)

$$\text{FT}\{r_s(t)\cos 2\pi f_c t\} = R_s(f) \otimes \left(\frac{1}{2}\delta(f-f_c) + \frac{1}{2}\delta(f+f_c)\right)$$

$$= I(f) \otimes \frac{1}{4T_s}\sum_{n=-\infty}^{\infty} \left(\delta(f-f_c-f_{IF}-nf_s) + \delta(f-f_c+f_{IF}-nf_s)\right.$$

$$\left. + \delta(f+f_c-f_{IF}-nf_s) + \delta(f+f_c+f_{IF}-nf_s)\right) \quad \text{(EQ 3.24)}$$

$$-Q(f) \otimes \frac{1}{4T_s}\sum_{n=-\infty}^{\infty} \left(\delta(f-f_c-f_{IF}-nf_s) - \delta(f-f_c+f_{IF}-nf_s)\right.$$

$$\left. + \delta(f+f_c-f_{IF}-nf_s) - \delta(f+f_c+f_{IF}-nf_s)\right).$$

The aim is to obtain a replica of I(f) at baseband and from equation (3.24), this requires that $f_{IF} - f_c = nf_s$ where m is any integer. Substituting this into equation (3.24) above

$$\text{FT}\{r_s(t)\cos 2\pi f_c t\}$$

$$= I(f) \otimes \frac{1}{4T_s}\sum_{n=-\infty}^{\infty} \left(\delta\left(f-\frac{f_s}{2}-(n+m)f_s\right) + \delta(f-(n-m)f_s)\right. \quad \text{(EQ 3.25)}$$

$$\left. + \delta(f-(n+m)f_s) + \delta\left(f+\frac{f_s}{2}-(n-m)f_s\right)\right)$$

$$-Q(f) \otimes \frac{1}{4T_s}\sum_{n=-\infty}^{\infty} \left(\delta\left(f-\frac{f_s}{2}-(n+m)f_s\right) - \delta(f-(n-m)f_s)\right.$$

$$\left. + \delta(f-(n+m)f_s) - \delta\left(f+\frac{f_s}{2}-(n-m)f_s\right)\right).$$

This can be simplified to give the desired results that

$$\begin{aligned} &FT\{r_s(t)\cos 2\pi f_c t\} \\ &= I(f) \otimes \frac{1}{4T_s}\sum_{k=-\infty}^{\infty}\left(2\delta(f-kf_s)+\delta(f-\frac{f_s}{2}-kf_s)+\delta(f+\frac{f_s}{2}-kf_s)\right) \\ &-Q(f) \otimes \frac{1}{4T_s}\sum_{k=-\infty}^{\infty}\delta(f-\frac{f_s}{2}-kf_s)-\delta(f+\frac{f_s}{2}-kf_s). \end{aligned} \qquad \text{(EQ 3.26)}$$

The same effect can be seen when $f_{IF} + f_c = mf_s$ and both conditions also hold for the extraction of $Q(f)$ at baseband. Therefore to summarize, the general relationship between f_{IF} and f_s is that $f_{IF} = mf_s \pm f_s/4$ (e.g 3/4 f_s, 5/4 f_s, 7/4 f_s, ...). This allows the sampling of a narrowband signal centred at a high IF with a sampling rate lower than the IF. This also implies that there are image bands separated in frequency from the desired signal by integer multiples of half the sub-sampling frequency where any interfering signal would also be "mixed" into the desired frequency band. Therefore the lower limit of f_s is also constrained by the effectiveness of the IF SAW filter.

3.3 DIRECT-DOWN CONVERSION

The basic architecture of a Direct-Down Conversion (DDC)receiver is illustrated in figure 3.4. The basic idea is to remove all the intermediate stages and therefore move most of the signal processing to the baseband as no channel selection is performed beforehand. The signal received at the antenna is mixed down to the baseband in one stage where it can then be sampled and processed digitally.

The advantages of this method are

- removing intermediate stages reduces component count therefore cost of parts and assembly decreased.

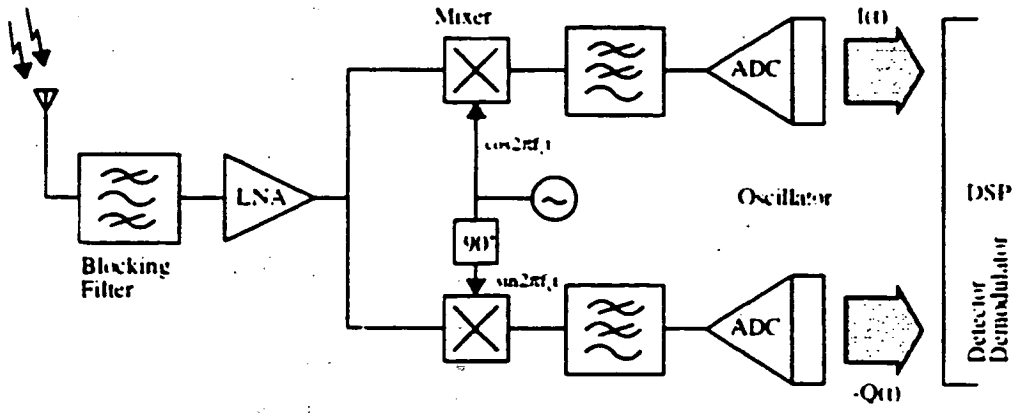


FIGURE 3.4 Direct-Down Conversion

- digital signal processing at baseband results in lower sampling rates where larger dynamic range converters are available.
- selectivity is performed at baseband where there are a wider range of circuit components that can be used due to the limited bandwidth.
- no RF image rejection filtering is necessary for frequency conversions directly to baseband (note that image bands caused by baseband sampling still occurs).

It should be pointed out here that the method of Direct-Down Conversion is not new and was proposed back in 1924 with the first patent being awarded in 1934 [26] however so far the superheterodyne structure has proven to be a better alternative with its multistage selectivity. The revival of interest towards DDC ([23], [24], [25], [26], [28], [29], [30], [31], [32], [33], [34]) has been caused by the improvements of signal processing, particularly in the digital domain together with the availability of large dynamic range ADC making channel selectivity possible at baseband.

There are 3 critical areas in determining a receivers performance, its selectivity, sensitivity and dynamic range and all high performance receivers are designed to achieve all three goals. In a superheterodyne receiver, the complexity is spread out amongst the various stages - as each stage becomes more selective, the dynamic range and sensitivity requirements of following stages can be reduced. The approach of the DDC is to shift the complexity to the baseband and somewhat also to the front-end stage and this has caused other associated problems

DC offset errors - there is a lot of gain at baseband in order to increase the sensitivity of the receiver to very weak signals. Any DC offset errors would be amplified immensely saturating circuitry and therefore must be removed. One solution is to use AC coupling in the analog paths. Another is to use digital processing to obtain a value of the DC offset and to use a digital-to-analog converter to produce a compensating DC signal to cancel the off-

set (this is increasing the complexity). The drawback of both solutions is that there is now a notch created at DC due to this filtering but because the desired signal spectrum is also at baseband, some useful information is also removed. In DECT where the signal is relatively wide-band (baseband bandwidth = .864 MHz) if a steep enough notch is created, the effect of the notch may be lessened.

- Flicker Noise (see Appendix B) - flicker noise is inversely proportional to frequency and therefore baseband circuitry are noisier thus to minimize this noise contribution, the RF front-end must have a higher gain (see equation (B15) in Appendix B) and the front of the baseband circuitry (baseband filter that performs the RF channel selection and high gain stage to reduce affects of noise of latter stages) must also be low-noise. However higher gains at DECT carrier frequencies become limited dependant upon the semiconductor technology used and LNA's and mixers designed with larger gains inherently become less linear resulting in a loss of linearity of the overall system (see Appendix B section B.2.1.2).
- Low frequency interference - in a DDC, because there is limited gain available from the RF circuitry, the baseband gain is rather large so as to improve the sensitivity of the receiver as well as reducing the susceptibility to noise from the following stages. However since the baseband bandwidth is 864 kHz, many low frequency interferers would be picked up by the baseband circuitry, particularly the broadcast from the AM radio band. To make matters worse, sufficient shielding of these low frequency signals may be difficult due to its great skin depth.
- Local Oscillator Feedthrough - Some of the oscillator's signal may leak through the mixer to the antenna and may then get reflected back towards the mixer which would then mix this down to DC. This DC offset may fluctuate as the reflection coefficient at the antenna changes with the physical positioning of the

hand or head with respect to the handset. Again if the fluctuations are slow, this effect can be reduced with the DC notch filtering. Also designs of the mixers with better mixer isolation and LNA's with larger reverse isolation helps.(see [23], [28]).

- Gain and Phase mismatch - as mentioned above these errors result in BER increases and therefore reduces the sensitivity of the receiver.
- Baseband Selectivity - if the baseband filter (see figure 3.4) is not capable of selecting a baseband channel then all the selectivity is performed by digital filtering. This may require a lot of computations since the order of the filter may be quite large and thus consumes power. The sampling rate may also be much larger that the nyquist rate so that aliasing does not occur. If selectivity is performed by the baseband filter then less digital filtering is required but this analog filter with its sharp cutoff will also consume some amount of power (sampling rate may be reduced as a benefit of analog filtering).
- Dynamic Range - the required dynamic range for DECT is 69 dB which translates to about 12 bits of resolution. The sampling rate would probably be several MHz thus the ADC would be quite power consuming and the computations at 12 bit resolution would also be quite demanding. To reduce the dynamic range, automatic gain control (AGC) circuitry is required after channel selection before the ADC and the estimation of the amplitude of the received signal would have to be [illegible] tal computation.
- Linearity [illegible] formed at baseband the linearity of the receiver for all the [illegible] selectivity must be linear to reduce intermodulation distortion. This would probably not be too much of a problem.

The only published DDC designed for DECT was by G. Schultes et al. [33],[34]. There architecture was basically the same as in figure 3.4 and included AGC to reduce the dynamic

range requirements after RF channel selection by an analog baseband filter. This reduces the resolution necessary in the ADC to 6 bits and with a sampling rate of 9.216 MHz, a flash converter was used which is rather power hungry (note that this DDC, two sets of ADC and high gain baseband stages are required because there is both an I and Q path). The baseband filter also provided the DC notch for AC coupling and was implemented as a 10 th order Butterworth filter (band-pass) so that the cutoff on both sides would be steep enough. This was implemented using operational amplifiers and thus required 5 of these amplifiers per filter for a total of 10 for the receiver (more power). The front-end used GaAs technology to reduce the noise figure of the system and also to obtain low intermodulation however the drawback to this is the cost of GaAs integrated circuits is still high compared to silicon and does not allow for the possibility of monolithic integration with the IF circuitry.

3.4 THE SINGLE IF DIGITAL QUADRATURE DEMODULATOR

The Single IF solution (see figure 3.5) eliminates many of the problems that occur in the Direct-Down Conversion architecture by down converting the desired signal to an IF frequency and then sampling the signal at this IF frequency as opposed to at baseband. Thus because the signal is converted to the digital domain at some intermediate frequency, the DC offset problem caused by local oscillator feedthrough and other circuit non-idealities is eliminated and the effects of flicker noise is also reduced (signal processing further away from DC). Quadrature sampling is also used and therefore removes gain and phase mismatch errors ([5], [35] and [36]).

The main difficulty with the implementation of this architecture is the value of the IF. A low IF would result in difficult image rejection at the RF frequency because of the close proximity of the image at RF (a frequency of 2 IF separates the image from the desired signal at RF). This is because the quality factor of the filters at 2 GHz are limited due to signal leakage and coupling at these high frequencies. Multiple IF stage architectures

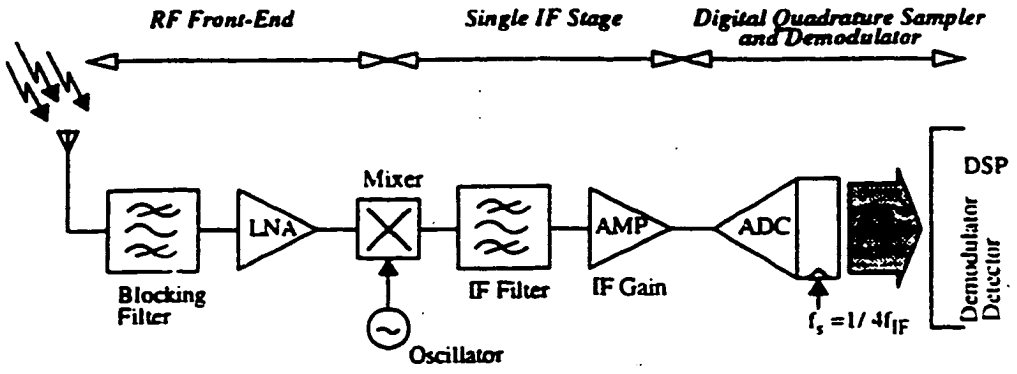


FIGURE 3.5 Single-IF receiver architecture

eliminate these problems. However a low IF is desired to keep sampling rates to a minimum and to simplify input circuitry to the ADC.

3.5 PROPOSED SYSTEM ARCHITECTURE

The proposed architecture for a DECT receiver illustrated in figure 3.6 is that of a single-IF Digital Quadrature Demodulator. Again the advantages of using a single-IF stage is that there will be fewer components to assembly in the manufacturing process which reduces costs and that power consumption is therefore also reduced. The benefits of digital demodulation immediately after the single-IF stage stem from digital signal processing. The hardware is more manufacturable because it can be produced with digital silicon technologies which tend to be more mature than their analog counterparts (fewer defects) and they are easier to test. This results in a higher yield which reduces costs. The density of circuitry is also greater in digital technologies minimizing silicon area (resulting in greater yields) or allowing for more complex signal processing per unit area increasing circuit integration and therefore reducing the component count necessary in assembly. With minimum feature sizes decreasing below half micron gate widths, the capacitance of the gate of the Metal-Oxide-Silicon (MOS) transistor required to switch current in digital circuits decreases and this results in lower power consumption. Another attraction to processing in the digital domain is the reduction in design time of these digital circuits through the use of digital cell libraries and synthesis tools. It should be noted here that like other digital quadrature demodulators, this architecture can be used to demodulate π/4-QPSK as well as GMSK with minimal modifications.

The key to this approach is the use of a Sigma-Delta analog-to-digital converter (ΣΔ-ADC) to perform the digital quadrature sub-sampling as opposed to conventional ADC's. The reasons for its use is again its manufacturability because of its high tolerance to fabrication process and circuit variations as well as the inherent linearity. The power consumption of the ΣΔ-ADC including decimation and low-pass filtering is also comparable or

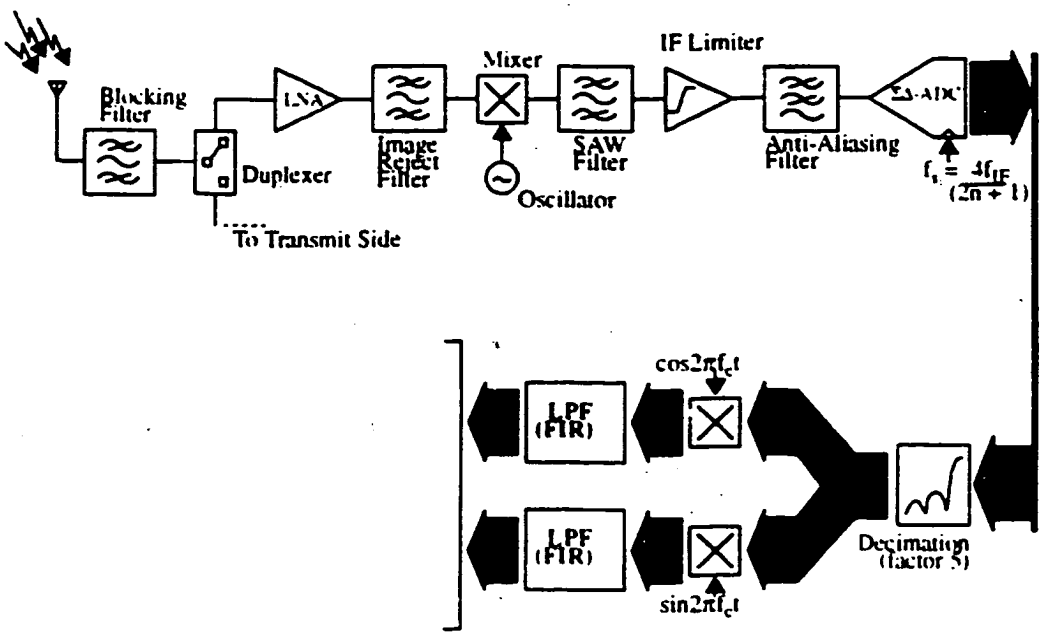


FIGURE 3.6 Single-IF receiver architecture with Sigma-Delta modulator

even better than certain conventional nyquist rate ADC's (at the same multi-bit conversion rates) and would probably decrease even more as digital silicon technologies move towards smaller feature sizes. This is the trade-off in using ΣΔ-ADC where a higher single-bit sampling rate (the over-sampled rate) is used resulting in a faster and simpler conversion from the analog to digital domain but this single-bit output requires further DSP (decimation and filtering) before it is useful. Thus because the cost in power and area of digital circuitry has significantly reduced. ΣΔ-ADC are becoming more attractive.

The design of this architecture also takes into account the intended fabrication technology that will be used to produce the integrated circuits. This is important because it allows the system to be designed so as to produce subsystem circuit specifications that are realistically achievable using that fabrication process. The target fabrication technology is a 0.8 micron Bipolar Complementary Metal-Oxide-Silicon (BiCMOS) process because of its ability to produce high-speed low-noise bipolar transistors for the RF and IF circuits as well as producing small MOS transistors for the digital circuits. Of course this can also be achieved by a high-speed bipolar silicon technology process used exclusively for the RF and IF circuits and a CMOS process for the digital circuits. Gallium Arsenide technology is not used because of its high costs at the present time (especially for the digital circuits) even though it is superior in performance at high frequencies.

3.5.1 RF Stage

The primary purpose of the RF stage is to produce enough gain with the minimal amount of noise added so as to keep the NF small while relaxing the noise requirements of subsequent stages. Selection of the band-of-interest (DECT band) is also necessary to eliminate out-of-band interference that may saturate the input circuitry. The signal is then mixed down to lower frequencies where signal processing is easier due to the availability of a wider range of circuits.

The first component in the RF stage following the antenna is a blocking filter (see figure 3.6). This is a bi-directional dielectric filter that blocks signals outside the DECT band during reception and also transmission by the wireless terminal. The Hitachi EF1890R2 was chosen because of its good selectivity and high attenuation at frequencies below 1 GHz. Its insertion loss is just under 2 dB which is common amongst these filters (see table 3.1 for the performance specifications). It is reasonably assumed that this filter is much more linear than the other active components in the architecture (particularly the LNA and mixer) because this is a passive device (which is also the reason why the NF is low).

The next component in the architecture is the duplexer which is a switch that connects the antenna either to the receiver chain or the transmitter chain. It is assumed that the insertion loss (IL) of the duplexer is 1 dB and that it is again much more linear than the LNA and mixer in the receiver and therefore is not the limiting factor in the overall linearity of the receiver.

Both the duplexer and the blocking filter is included in the receiver analysis because they attenuate the signal before the first amplifying component (LNA) and thus contributes significantly to the overall NF and sensitivity of the receiver. They are present in most cordless and cellular architectures.

The LNA was custom designed for this application because at that time there were no commercially available amplifiers that used a 3 V power supply. Before finally determining the specifications for this component, circuit simulations of various different LNAs were made and then they were fabricated to deduce the limits of the silicon technology. A LNA was then designed that compromised between the various conflicting demands on the NF, TOI and power consumption resulting in the following specification:

- NF = 5.4 dB
- OIP3 = 2.5 dBm
- Gain = 18.5 dB

f_0 [MHz]	Bandwidth [$f_0 \pm$ MHz]	Insertion Loss [dB max]	Ripple [dB max]	VSWR	Selectivity [dB min (at MHz)]
1890.0	10.0	2.0	1.0	2.0	12, 40 (f_0 - 40, 220)

TABLE 3.1 Specification for Hitachi EF1890R2 Dielectric Filter

The mixer was also custom designed for the same reasons and resulted in the following specifications.

- NF = 17 dB
- OIP3 = 16 dBm
- Gain = 10 dB

Further details of these designs are presented in chapter 5.

In between the LNA and the Mixer there is an image-reject filter. The purpose of this filter is 2 fold. First, there must be enough interference attenuation at the image frequency from the mixing in the RF stage. This is because an out-of-band signal at the image frequency can have a signal strength of up to -23 dBm for a desired signal power level of -80 dBm (see section 2.3.5.7). Thus in order to obtain the required SNR of about 14 dB (see section 2.3.5.5) there must be an attenuation of at least 71 dB. The first ceramic filter (before the duplexer) provides for 40 dB of attenuation (see table 3.1) at an image frequency of 1670 MHz and thus another Hitachi EF1890R2 would be sufficient. This implies that the first IF frequency of this receiver architecture has to be at least about 100 MHz (if the IF frequency is smaller, the image frequency becomes closer to the band-of-interest and results in less attenuation of the image). Note that if the attenuation of the first ceramic filter at the image frequency of 1670 MHz is at least 71 dB then the second image-reject filter is not necessary as the -21 dBm interferer has already been adequately diminished (alternatively choose a higher IF corresponding to a larger difference between the image frequency and band-of-interest and thus a greater image attenuation for the same frequency). However the other reason for image rejection after the LNA is to attenuate the noise added by this amplifier (stages before the LNA do not affect the noise added by the LNA alone) at the image frequency because this noise band will also be mixed into the IF band by the mixer. This has the same effect of increasing the NF of the LNA by 3 dB.

One possible alternative is for the first ceramic filter to have an attenuation of at least 56 dBm at the image frequency and to design an image-reject mixer with image rejection of about 15 dB (presently achievable in practice). The image rejection of the mixer is achieved through circuit design and therefore requires no filter to be inserted between the LNA and mixer with added advantages of not requiring a 50 ohm buffered output from the LNA directly into the mixer saving power. However from the ceramic filters investigated so far (Hitachi, Panasonic, Murata Erie) the Hitachi filter had the best attenuation. To achieve the required attenuation the IF would have to be higher but this (as explained below) is not desirable.

It is assumed that a suitable oscillator can be found.

3.5.2 IF Stage

The primary purpose of the IF stage is to provide enough gain before the ADC. This is because the conversion to the digital domain results in quantization errors from the finite number of bits used to represent the signal magnitude and that effectively adds a lot of noise to the signal. Thus the NF of ADCs is rather large compared to other components in the receiver chain. To prevent this noise from deteriorating the SNR of the receiver, the desired signal level must be increased before the ADC and results in the need for a large gain in the IF stage. This is equivalent to having a large gain G_1 in equation (B15) of appendix B to mask the effects of a large noise factor F_2 on the overall noise factor F. Since the quantization noise added by an ADC is inversely proportional to the ADC's resolution in bits (see section 3.5.4), then in order to reduce the resolution to save power (fewer bits means fewer digital computations) and decrease the ADC complexity, a larger IF gain is required.

The need for large gain always conflicts with the linearity and power consumption requirements. Table 3.2 provides the performance specifications of some commercially available linear amplifiers for operation at about 100 MHz.

Product	Gain [dB]	NF [dB]	OIP3 [dBm]	Supply Current [mA]	Conditions
Avantek INA-01170	32.5	1.7	23	35	f = 100 MHz Vcc = 5.5V
Avantek MSA-0685	20	2.9	14.5	16	f = 100 MHz Vcc = 3.5V
Avantek MSA-0800	32.5	2.8	27	36	f = 100 MHz Vcc = 7.8V
Avantek IVA-05200	30	9	7	35	f = 500 MHz Vcc = 5V
Philips NE/SA5205A	19	5.8	9	19	f = 100 MHz Vcc = 5V
Philips NE/SA5219	13	9.5	13.5	43	f = 100 MHz Vcc = 5V
Plessey SL6140	15	-	-	19	f = 100 MHz Vcc = 12 V

TABLE 3.2 Commercial specifications of some IF amplifiers operating at 100 MHz

It is estimated that an IF gain of at least 60 dB is needed which requires cascading a minimum of 2 of these amplifiers, however this significantly reduces the IIP3 of the combined stages (see section 2.1.2 of appendix B) because of the high gains involved with the second stage limiting the overall linearity (e.g. OIP3 of 2 cascaded MSA-0800 is 27 dBm therefore IIP3 is 27 - 2(32.5) = -38 dBm). This does not meet the required IIP3 of -20.6 dBm and would require filtering in-between the 2 amplifiers to remove the intermodulation distortion caused by this lack of linearity. Also of great concern is the power consumption of these amplifiers and it appears that using three Avantek MSA-0685 would be the most power efficient but that would still consume 48 mA of current although the voltage supply is below 5V.

Large gain linear amplification at the IF frequency of about 100 MHz is therefore not suitable for this architecture. The solution is to first select a single DECT RF channel at the IF and then amplify this signal with a limiting amplifier. This type of non-linear amplifier achieves a very large gain without needing to consume a lot of power by sacrificing its linearity however the linearity requirements, after frequency selectivity, are extremely relaxed because only the desired channel is present as all other in-band interferers have already been severely attenuated in the selection process so that their intermodulation products are negligible. An example of a limiting amplifier designed to operate around the 110 MHz is found in National Semiconductor's LMX 2240 (see table 3.3 and figure 3.7)

Notice that for the any IF signal above -80 dBm appearing at its input, the amplitude of the output signal is always 1V thus all the amplitude information is lost after this component and therefore non-linear amplifiers can only be used to demodulate signals whose amplitudes carry no information about the data being conveyed (i.e constant envelope modulation schemes which includes GMSK and $\pi/4$-QPSK). There is also an output signal from this amplifier that is proportional to the signal power at its input, the Received Signal Strength Indicator or RSSI (common in most limiting amplifiers). This is necessary be-

Gain [dB]	NF [dB]	Input Impedance [Ω]	Output Impedance[Ω]	Supply Current [mA]	Conditions
70	7	150	100	8	Vcc = 3V

TABLE 3.3 Performance Specification for Limiter in LMX 2240 at 100 MHz

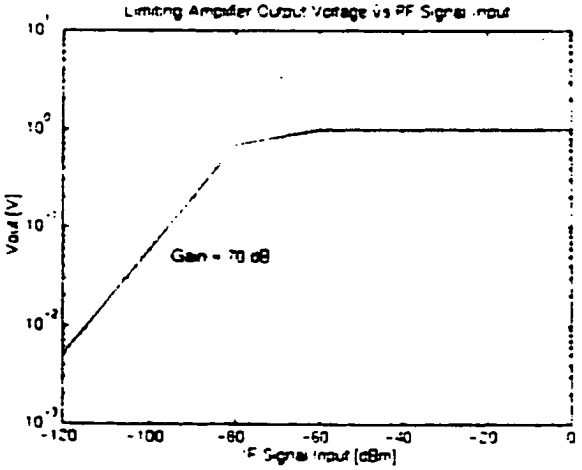


FIGURE 3.7 Gain of LMX 2240 at 110 MHz

cause DECT requires this signal strength measurement in deciding which channel is the clearest (see section 2.3.2 - 2.3.4). The upper frequency limit of the input signal for this amplifier is 150 MHz which therefore is the upper limit for value of the IF.

The selectivity at this IF is performed by a Surface Acoustic Wave (SAW) filter because of its high quality factor (bandwidth of 1.728 MHz), passing only one RF channel and attenuating all the other DECT channels (see figure 3.8). It is also very stable with temperature, can be designed to have reasonably linear group delay characteristics in the pass band and is passive therefore consumes no power. There are many SAW filters available designed for DECT applications from many different manufacturers (e.g Sawtek, Toko, Murata Erie) all with a centre frequency of 110.592 MHz. This centre frequency was chosen by a group consisting of component and equipment manufacturers working for European Community Telecommunications (ECTEL) to standardize key component specifications for DECT before the DECT standard was finalized and is not specified in the standard as the value for the IF (no value is given in the standard as this not part of the standard). This value 110.592 MHz is shown in section 3.5.5 to be not suitable for the architecture being proposed and a custom built SAW filter would have to be used. Presently, there is a custom SAW built for DECT available for this research with a centre frequency of 103.68 MHz and this value is in the set of frequencies computed in section 3.5.5 that can be used in this receiver. Since a custom SAW filter is required, it is possible to select any of the allowable IF frequencies computed in that section as the centre frequency of the filter, however a frequency close to 110.592 MHz would be prudent so that other components developed using the specifications from the ECTEL group can be used (including the LMX 2240). Also, choosing IF frequencies lower than 100 MHz results in more difficulty in image rejection (see section 3.5.1) and larger SAW filters.

The disadvantages of using SAW filters with these centre frequency and bandwidth requirements is that they would have to have a transversal filter structure which commonly

has an insertion loss of greater than 10 dB. The gains of the LNA and mixer must therefore be higher to compensate for this and to maintain the overall system NF. The costs of these filters are about $10, approximately 5 - 10% of the target cost of a portable terminal however there are no other convenient replacements for these filters in radios. Care must be taken when interfacing circuit components to some SAW filters as the assumption that their input and output impedances are 50 Ω may be erroneous.

The SAW filter and limiting amplifier are followed by a low pass filter whose function is to remove the distortion caused by the limiting amplifier on the desired signal. The effect of the limiting amplifier on a GMSK signal is illustrated in figure 3.9 (noise floor was limited by number of sampling points used in the Fast Fourier Transform - FFT). Distorted signals are created at the odd harmonics of the IF frequency thus low-pass filtering is required to remove them in order to recover the uncorrupted GMSK signal at the IF frequency (a simple 4th order filter made from passive elements would be sufficient to attenuate the distortion to at least 50 dB below the desired GMSK signal). This intuitively makes sense because, if in the limit, the frequency deviation of the GMSK signal at the IF is much smaller than the IF then the signal can be represented as a single tone and large amplification of a single tone followed by limiting its amplitude results in approximately a square wave which contains many odd harmonics.

3.5.3 Baseband Sampling Rate and Clock Recovery

The sampling frequency of the baseband I and Q signals (the multi-bit sampling rate at baseband) determines the over-sampling rate of the ΣΔ-ADC which in turn determines the intermediate frequency (see section 3.2.4). Recall that the knowledge of I(t) and Q(t) allows for the computation of the instantaneous phase (see equation (3.5)). If the receiver was in exact synchronization with the received GMSK signal then all that is required for demodulation is the knowledge of the instantaneous phase at current symbol time ($\varphi(kT_b)$ where T_b = one bit period and k is the current bit number) the phase at the previous sym-

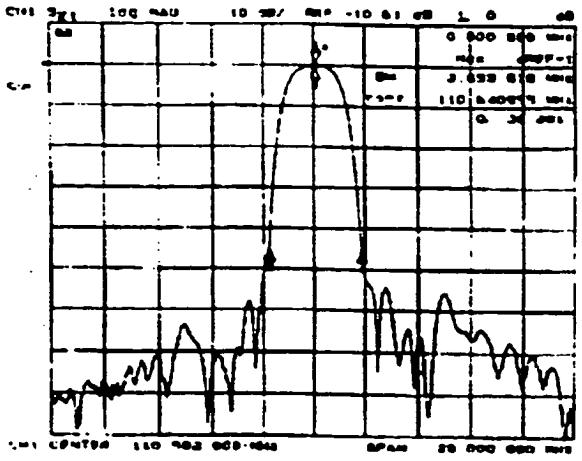


FIGURE 3.8 Frequency response of SAWTEK SAW filter (part number 854361)

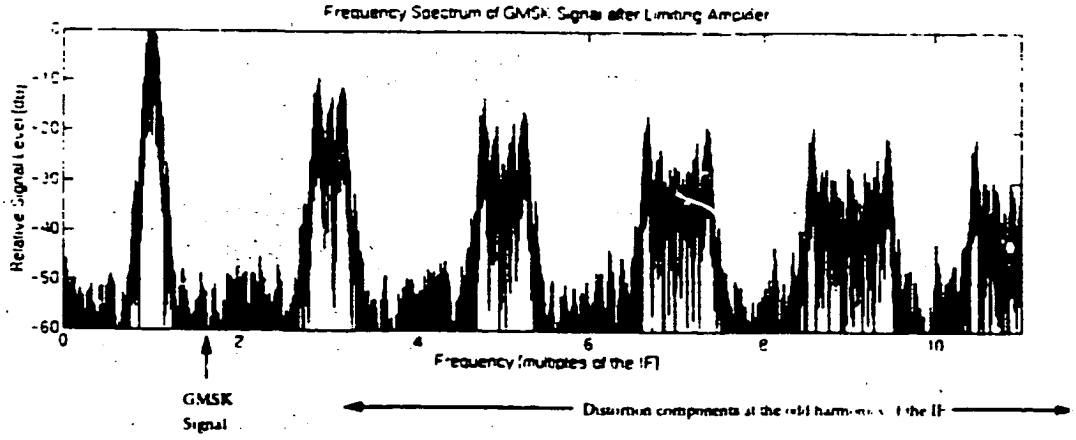


FIGURE 3.9 Effects of hard-limiting on a GMSK signal

bol time ($\varphi([k-1]T_b)$) and the value of the previous data bit. The difference in the phase is proportional to the sum of these 2 data [illegible] urrent and previous) encoded in Non-Return to Zero (NRZ) format (i.e 1 or -1). Thus when synchronized, one sample per data bit at the symbol time ($t = kT_b$) is sufficient. However, the receiver is not in bit synchronization with the signal initially and thus more samples per data bit is required. If seven samples are taken per bit period, the sensitivity would be decreased by less than 1 dB (see [33]). The sampling rate at baseband is therefore set at 8 times the data bit rate (9.216 MHz). The data clock can now be recovered (see [37]) by determining at which sampling point out of the 8 in one data bit period the difference in phase ($\varphi(kT_b) - \varphi([k-1]T_b)$) is at its maximum absolute value (note that this only occurs during data symbol transitions).

3.5.4 Quantization Noise and Baseband Bit Resolution

Sampling of any signal and the conversion to the digital domain results in quantization errors due to the finite number of bits available to represent the signal magnitude. This effect can be considered as an additive random noise signal that represents the error between the actual signal magnitude and its quantized value at that sampling instance. In order to maintain the required sensitivity of the receiver, this quantization noise must be much lower than the minimum detectable signal. Intuitively, the fewer the number of bits of resolution, the greater the quantization noise therefore to achieve a certain SNR, the preceding stages must have a greater gain so that the NF of the system is not drastically increased due to this added noise (see equation (B15) in Appendix B).

An approximation of the NF of an n-bit ADC [36] can be computed from the following (assume the noise in the ADC is mainly from the quantization effect - valid for low bit resolutions).

Let,

- error produced by quantization (e) = signal magnitude - quantized signal magnitude.
- [-Vq, Vq) is the voltage range of the A/D at the input.

Therefore (if no limiting occurs)

$$|e| \le \frac{1}{2} \cdot \left(\frac{2V_q}{2^n}\right) = \frac{V_q}{2^n}. \qquad \text{(EQ 3.27)}$$

Now assuming the probability density function of the random variable e (p(e)) is uniform then

$$p(e) = \begin{cases} \dfrac{1}{2V_q/2^n} = \dfrac{2^{n-1}}{V_q} & \text{for} \quad |e| \le \dfrac{V_q}{2^n} \\ 0 & \text{otherwise} \end{cases} \qquad \text{(EQ 3.28)}$$

Therefore the mean of the error E{e} = 0 and the variance

$$\sigma_e^2 = E\{e - E\{e\}\} = E\{e^2\} = \int_{\frac{-V_q}{2^n}}^{\frac{V_q}{2^n}} e^2 \left(\frac{2^{n-1}}{V_q}\right) de = \frac{V_q^2}{3(2^{2n})}. \qquad \text{(EQ 3.29)}$$

Now the autocorrelation of the sampled noise is

$$E\{e[n]e[n+\tau]\} = \begin{cases} 0 & \text{if } |\tau| > 0 \text{ assuming } e[n] \text{ uncorrelated} \\ E\{e^2[n]\} = \sigma_e^2 & \text{if} \quad \tau = 0 \end{cases}$$

$$\Rightarrow R_e[\tau] = E\{e[n]e[n+\tau]\} = \begin{cases} \sigma_e^2 & \text{if} \quad \tau = 0 \\ 0 & \text{else} \end{cases} \qquad \text{(EQ 3.30)}$$

thus the spectral density is the discrete Fourier transform of the autocorrelation

$$N(z) = \sum_{\tau=-\infty}^{\infty} R_e[\tau] z^{-\tau} = \sigma_e^2. \qquad \text{(EQ 3.31)}$$

This is in the Z domain therefore in the frequency domain this becomes (see [59] pp 87)

$$N(f) = T_s\sigma_e^2 = \frac{2V_q^2}{3f_s 2^{2n}} \qquad \text{for } |f| \le \frac{f_s}{2} \qquad \text{(EQ 3.32)}$$

where $f_s = 1/T_s$ is the conversion rate into the n-bit samples.

Now if the input impedance of the ADC is R ohms then the noise power density is

$$N(f) = \frac{2V_q^2}{3f_s 2^{2n} R} \quad \left[\frac{W}{Hz}\right] \qquad \text{for } |f| \le \frac{f_s}{2}. \qquad \text{(EQ 3.33)}$$

From equation (B7) and the definition of the NF given in (B9) of Appendix B, the NF of the ADC (assuming matched conditions) is

$$NF = 10 \cdot \log\left(\frac{kT + N(f)}{kT}\right) = 10 \cdot \log\left(1 + \frac{2V_q^2}{3f_s 2^{2n} kTR}\right) \qquad \text{(EQ 3.34)}$$

where k is Boltzmann's constant ($1.38\ (10^{-23})$ J/K) and T is the temperature in Kelvin (normally T = 290 K for room temperature). For example, the NF at room temperature of a 6 bit ADC (n = 6) with a sampling rate of f_{conv} = 9.216 MHz, an input impedance of R = 100 Ω and voltage magnitude range of V_q = 1 is 76.5 dB.

Keeping to this ADC, the cumulative NF and IIP3 (equations (B16) and (B28) in Appendix B) values can be computed for the overall system and the results are presented in table 3.4. The linearity before the SAW filter is -14 dBm (referred to the input) exceeding the requirements from the standard and is mainly restricted by the LNA. The linearity of the system after the SAW filter is of less concern because of the selectivity of the SAW (as explained above) and because the components after the limiting amplifier are reasonably linear (a 1 bit ΣΔ-ADC is inherently linear). The overall NF is 9.9 dB and this is also well

below the maximum NF allowed by DECT (16.8 dB) which only requires the ADC to have 3-bit resolution but this leaves no safety margin. With a 3 dB noise margin, the required resolution is 4 bits but for a realistic and practical product, the safety margin afforded by using 6 bits of resolution is more prudent. Also if only 4-bits of resolution is used, the maximum SNR of the receiver will be 24 dB and thus the residual BER (BER at high signal levels) will be restricted by this.

3.5.5 Over-Sampling Rate of the Sigma-Delta Converter

The over-sampling rate of the ΣΔ-ADC is related to the IF by the expression given in section 3.2.4. It also has to be a multiple of the baseband sampling rate (9.216 MHz) so that the decimation factor for sampling rate reduction to 9.216 MHz is just an integer making decimation easier. Finally, this over-sampling rate has to be large enough so that the quantization noise introduced in the analog-to-digital conversion process does not affect the overall system NF and sensitivity (see the next chapter for details).

It has already been deduced in the previous section that a 6 bit resolution is required at the baseband sampling rate. Therefore the SNR of the band-pass ΣΔ-ADC in the band of interest must be at least 36 dB. For these band-pass ΣΔ-ADC, the SNR increases approximately by 3k + 3 dB for each octave increase in the over-sampling rate (see [38]) where k is the order of the modulator (for a low-pass ΣΔ-ADC, the increase in SNR per octave is 6k + 3). Thus the over-sampling rate of the ΣΔ-ADC can be decreased by increasing the order k of the ΣΔ modulator but this results in an increase in the complexity of the ΣΔ-ADC (the ΣΔ-ADC can be thought of as a filter of order k thus increasing k improves this filters frequency response to the quantization noise it is trying to filter out but circuitry becomes more complex) and therefore would not necessary improve the power consumption of the ADC. A sixth-order modulator appears to be a good compromise between complexity and the sampling rate (4th-order modulators result sampling rates that are approximately double that of the 6th-order ADCs and high sampling rates not only increases power

consumption but also increase circuit complexity too). For a SNR of 36 dB, the 6th-order ADC requires an oversampling rate of about at least 40 MHz.

The possible set of values for the IF frequency (f_{IF}) can now be deduced from the following conditions that were explained above

Definitions:

f_{IF} = IF frequency

f_{os} = over-sampling rate of band-pass $\Sigma\Delta$-ADC

f_{conv} = baseband conversion rate (6-bit resolution)

f_{bit} = data bit rate = 1.152 Mbps

Z = set of integers

Conditions:

$f_{conv} = M \cdot f_{bit}$ where $M \geq 7, M \in Z$

$f_{os} = 4 \cdot f_{IF}/(2n + 1)$ where $n \in Z$

$f_{os} = D \cdot f_{conv}$ where $D \in Z$

$f_{os} > 40$ MHz $\Rightarrow M \cdot D \geq 35, M \cdot D \in Z$

100 MHz $< f_{IF} <$ 120 MHz

The over-sampling rate (f_{os}) and IF frequency (f_{IF}) is determined using these conditions in chapter 4.

3.6 CONCLUSION

A DECT receiver architecture has been presented here that has only one IF stage at about 100 MHz which reduces the component count and cost compared to a multi-IF superheterodyne structure. The retained IF stage reduces the higher gain and therefore linearity requirements on the RF front-end of a DDC and also eliminates the contradicting demand that the baseband circuitry be low-noise. Another major drawback of the DDC is that because a high baseband gain is necessary, any baseband noise can be coupled in and amplified reducing the receiver's sensitivity. This is particularly relevant in a DECT receiver

	INDIVIDUAL			CUMULATIVE			
Component	Gain [dB]	NF [dB]	OIP3 [dBm]	Gain [dB]	NF [dB]	OIP3 [dBm]	IIP3 [dBm]
Ceramic Filter	-2	2	100	-2	1.0	100	102
Duplexor	-1	1	40	-3	2.2	40	43
LNA	18.5	5.4	2.5	15.5	8.2	2.5	-13
Ceramic Filter	-2	1	100	13.5	8.2	0.5	-13
Mixer	10	17	16	23.5	9.4	9.4	-14
SAW	-12.5	4	100	11.0	9.4	-3.1	-14.1
Limiting Amplifier	70	8	-	81.0	9.6	-	-
LPF	-2	2	100	79.0	9.6	-	-
ADC	-	77	-	-	9.9	-	-

TABLE 3.4 Link Budget for DECT Receiver

since the DECT baseband circuitry bandwidth is 864 KHz, and this covers the lower range of the AM broadcast band.

The receiver consists of a low-noise RF front-end that amplifies and mixes the desired signal in the DECT band to the IF frequency by applying the correct LO frequency into the RF mixer. The DECT band is selected by the combination of the blocking filter and the image-reject filter. The DECT RF channel is then selected by the SAW filter that has a band-pass response with a DECT RF channel bandwidth and then amplified by the IF limiter. The gain of this limiter allows the following stages to be noisier without impairing the overall noise performance of the system. Thus a low-resolution ADC can be used to sample the signal at this point.

Using parameters from commercially available components for the blocking and image-reject filter (ceramic filter), duplexor, SAW filter and limiting amplifier, and also parameters for the RF front-end LNA and mixer that were realizable in the silicon process with which these components were made from (see chapter 4), the sensitivity and intermodulation performance was found to meet the DECT requirements by computing the NF and IIP3 of the overall receiver (see table 3.4).

The single-IF architecture involves using a BPΣΔM to sub-sample the IF signal and it will be shown in chapter 4 that by careful choice of the over-sampling rate and IF frequency, the in-phase and quadrature components can be easily separated by simply alternating the sign of the 1-bit output of the BPΣΔM before decimation which greatly simplifies the quadrature demodulation process as a 1-bit inversion at the over-sampled rate is still less demanding with respect to computations and power than for example a 6-bit multiplication at the baseband conversion rate of 9.216 MHz (8 times the data symbol rate).

CHAPTER 4

BAND-PASS SIGMA DELTA MODULATOR FOR DECT RECEIVER

4.1 INTRODUCTION

Analog-to-Digital conversion is now very common in modern digital receiver architectures because once the received information has been converted into the digital domain, the information that was sent can be recovered using digital signal processing which is both easier to design and simulate as well as easier to manufacture and reproduce with great consistency. By programming the digital signal processor differently, different demodulation schemes and filters can be implemented without changing the hardware giving the baseband processing hardware much flexibility.

Ideally, the earlier the conversion to the digital domain takes place in the receiver chain, the sooner the benefits of digital processing in the receiver occurs however analog-to-digital conversion normally takes place at baseband frequencies (less than 10 MHz). This is because the use of analog-to-digital converters has been restricted to those with lower conversion rates as higher rate samplers consume more power (upto to several Watts for Flash converters operating at several tens of MHz). For the bandlimited signal in a DECT RF channel (bandwidth = 1.728 MHz) that has already been down-converted by the RF mixer to its IF frequency of about 100 MHz, it is not necessary to sample the signal at twice the IF frequency. Theoretically, a bandlimited signal need only be sampled at rate equivalent to its bandwidth in order to ensure that the signal is not distorted by aliasing, and in chapter 3, a relationship between f_{IF} and f_s was established that sub-sampled a bandlimited signal such that not only was the sampling rate less than the IF frequency but the sampled signal could then be easily separated into its in-phase and quadrature components by a change of sign (quadrature sub-sampling). However, the lower limit of the sub-sampling

rate was shown not only to be restricted by the bandwidth of the signal to be sampled but also by the image bands that sampling creates and with quadrature sub-sampling, these image bands are separated in frequency from the desired signal by integer multiples of half the sub-sampling frequency. Thus the analog-to-digital converter must still have a reasonably high sampling rate (tens of MHz).

Sigma-Delta analog-to-digital converters have inherently high sampling rate but do not require as much power. This type of converter works by limiting the bandwidth of a signal that is to be sampled to a very narrow band and pushes most of the quantization noise to the wide out-of-band regions therefore retaining the desired in-band SNR. Initial applications restricted this sampling frequency band of inputs to baseband frequencies however this has now been expanded such that the input frequency band can be customized to higher centre frequencies producing a high frequency narrowband analog-to-digital converter. The 1-bit output from the Sigma-Delta modulator is also ideal for the quadrature separation process (multiplying by sine or cosine - see chapter 3) as this operation simplifies to that of a 1-bit inverter. The higher sampling rate also allows for more relaxed component tolerances in the design and manufacturing of it. Thus this kind of converter appears to be most suited for extending the digital domain to higher frequency stages of narrow band receiver as a quadrature sub-sampler.

This chapter begins with a brief discussion on sigma-delta modulators and demonstrates the basic compromises between complexity, over-sampling rate and the input signal bandwidth on the SNR performance but defers the tasks of providing more detailed information to the published literature in the listed references. The transfer function of the ΣΔM is then determined that minimizes the noise in a 1.728 MHz band (bandwidth of a DECT RF channel) centered at one fourth the over-sampling rate using the Cascade-of-Resonator architecture first developed by Schreier and Snelgrove [38] and the system specifications from chapter 3. Various time domain simulation in MATLAB using a GMSK input were

then performed to determine the exact IF frequency and over-sampling rate, the Cascaded-Integrator-Comb (CIC) decimator and the baseband FIR filter (used to suppress the quantization noise from the ΣΔM and CIC decimator). The bit-error rate performance was then simulated by demodulating the baseband in-phase and quadrature output from a GMSK input in a non-fading static additive white Gaussian noise (AWGN) environment.

It is noted here that this type of BPΣΔM capable of sub-sampling a narrow band signal centred at about 1.25 MHz at an over-sampling rate of about 50 MHz is to the author's knowledge not available, however a low-pass ΣΔM operating at an over-sampling rate of 50 MHz consuming only 41 mW (power does not include decimation/baseband filter circuits) and constructed using switched-capacitor circuit techniques in 1 μm CMOS technology has already been reported some time ago [52] and with advances in CMOS and BiCMOS technologies (smaller feature sizes) faster switching circuitry will be achievable [54]. Also, these types of modulators can be built using circuit techniques other than switched-capacitor. However, CMOS or BiCMOS technologies allow for higher levels of integration and with smaller feature sizes, the charging capacitance of a CMOS gate decreases resulting in not only faster switching times but a savings in power (for the same sampling rate but larger gate capacitance) [79].

The purpose of this chapter is not to provide a detailed circuit implementation of a BPΣ–ΔADC but to determine through high-level analysis the necessary frequency response (transfer function) based on a possible architecture, demonstrate through Matlab simulations without taking into account circuit non-idealities, that the modulator and decimator does indeed provide the expected representation of a GMSK signal and that this can be achieved within a reasonable dissipation of power.

4.2 SIGMA-DELTA MODULATOR BASICS

The purpose of this section is to present the fundamentals of ΣΔ modulation using a first-order ΣΔ modulator as an example. This is then followed by discussions of higher order modulators and finally using these established basics, bandpass ΣΔ modulators are described.

4.2.1 Delta modulation

The Delta modulator is shown in figure 4.1. From this figure it is obvious that the feedback loop causes g(t) to track x(t) where e(t) is the error signal computed from the difference in x(t) and g(t) (the estimate of x(t)). y(t) is the quantized sampled representation of e(t) after the 1-bit quantizer which makes a decision (positive or negative) every T_{OS}. Thus y(t) is the quantized rate of change of x(t) and hence the name Delta Modulation. To reconstruct x(t) from y(t), as in for g(t), y(t) must be put through an integrator (accumulator) and then low-pass filtered to remove replication from the sampling process as shown in figure 4.2. This is referred to as pulse-density modulation since, for example, if the number of positive pulses in a sample window (density of positive pulses) is greater than the number of negative pulses then the slope of x(t) is positive.

4.2.2 First-Order Sigma-Delta Modulator.

A first-order ΣΔ modulator has an integrating block (accumulator) before the delta modulator (see figure 4.3). The integrating block serves not only to simplify the demodulation process but also reduces the required slew-rate of the system because the signal presented to the delta modulator block is the integral of the input signal and therefore has a smaller slew-rate.

From the previous discussion on the Delta modulator, y(t) represents the rate of change of x'(t) with time. Now x'(t) is proportional to the integral of x(t) with respect to time thus y(t) provides an estimate of x(t) after low-pass filtering.

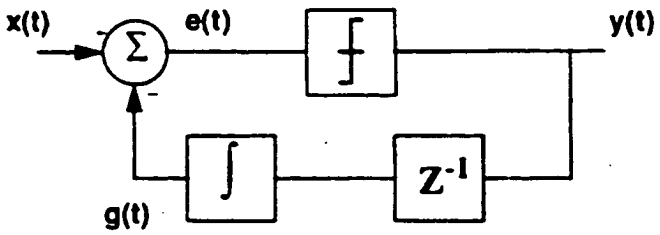


FIGURE 4.1 Delta Modulator

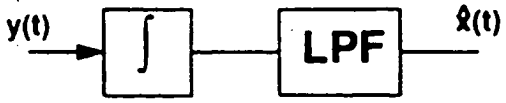


FIGURE 4.2 Reconstruction from Delta Modulator

This modulator is a non-linear system because of the quantizer however an approximation of the quantizer as a noise source contributor to its input allows for linear Z-domain analysis of this linearized model of the modulator which reveals with sufficient accuracy certain properties of ΣΔ modulators. The major assumption that has to be made is the statistical distribution of this quantization noise. It will be assumed here that the distribution of the noise is normal (white noise) which implies that the quantization errors are uncorrelated and independent of each other [84]. For a single loop (first-order) ΣΔ modulator, this has been shown to be not true [39] but rather coloured [40,41,42]. However for higher order ΣΔ modulator with binary quantizers, the quantization noise is white [40,43] and therefore since the derivations used here are to be extended to higher order modulators, this assumption is used. The noise becomes more uncorrelated with more feedback loops.

The linearized model of a first-order ΣΔ modulator is shown in figure 4.4. The 2 integrating blocks of the modulator have been moved inside the feedback loop. The relationship between the signal x(t) and the output y(t) (the signal transfer function - STF) is given by

$$STF(z) = \frac{Y(z)}{X(z)} = z^{-1}. \qquad \text{(EQ 4.1)}$$

The transfer function between the quantization noise and the output (the noise transfer function - NTF) is

$$NTF(z) = \frac{Y(z)}{Q(z)} = (1 - z^{-1}). \qquad \text{(EQ 4.2)}$$

In the frequency domain the STF is an all pass function whereas the power of the quantization noise is altered in magnitude by the squared magnitude of the NTF

$$|NTF(f)|^2 = |NTF(z)|^2\Big|_{z = e^{j2\pi f/f_{os}}} = 4\sin^2\left(\frac{\pi f}{f_{os}}\right). \qquad \text{(EQ 4.3)}$$

For small values of f, this can be approximated by $4(\pi f/f_{os})^2$ which is attenuating at low frequencies, and for f approaching f_{os}, there is a gain in noise power of 4. Since the quan-

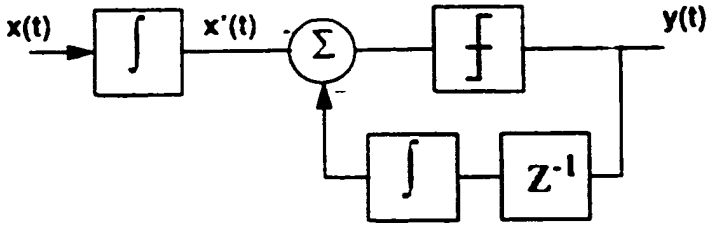


FIGURE 4.3 First-order Sigma-Delta modulator

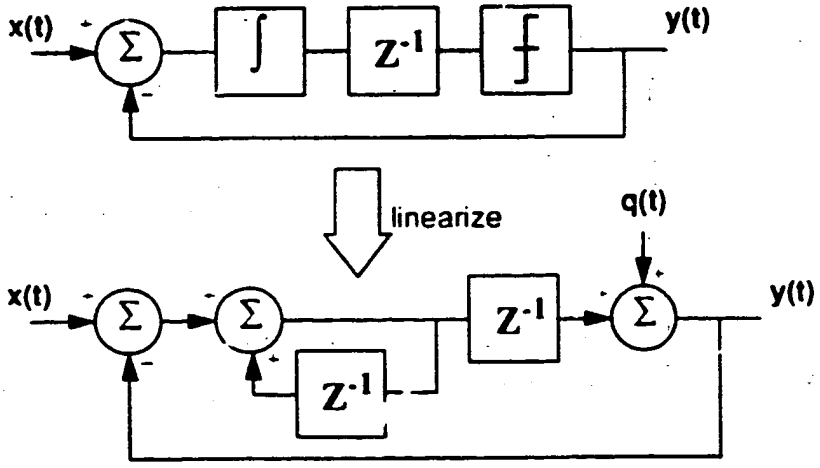


FIGURE 4.4 First-order Sigma-Delta modulator

tization noise spectrum is assumed to be white then this NTF has the effect of moving the noise power from the low frequencies to the high frequencies and therefore if the desired signal spectrum (X(f)) consists of relatively low frequencies compared to the sampling rate f_{OS} then the SNR there will be large due to the attenuated output noise power for $f << f_{OS}$. Thus the spectrum of y(t) consists of the shaped noise spectrum and desired signal spectrum at baseband (see figure 4.5) and to recover x(t) while retaining the SNR, a low-pass filter must be used to attenuate the high frequency noise decimation may also be performed to reduce the sampling rate.

This also illustrates how, implicit to the use of ΣΔ modulators is the fact that the x(t) is normally a narrow-band signal (and in this case at baseband) and that in order to achieve the necessary SNR, the sampling rate of the modulator f_{OS} has to be relatively large (hence f_{OS} is referred to as the over-sampled frequency). This is the trade off between the required analog precision circuit elements in conventional A/D converters and the higher sampling rates in the ΣΔ A/D converters. The next section describes how higher order modulators can reduce the required over-sampled frequency.

4.2.3 Higher Order Sigma-Delta Modulators

There are many different architectures that increases the order of ΣΔ modulators which in turn increases the noise shaping abilities.

The multistage noise shaping (MASH) modulator was introduced by K. Uchimura et al. [44] and involved using a single-order ΣΔ loop to requantize the quantization noise of the first single-order ΣΔ modulator. By carefully matching transfer functions within these loops, the quantization noise from the first loop can be cancelled. One advantage of using this architecture is that only single-order loops are involved that are not nested therefore because a single-loop is unconditionally stable (phase shift within feedback never becomes greater than π) the complete system remains stable. However the misgivings are that some matching of transfer functions are required which puts more constraints on com-

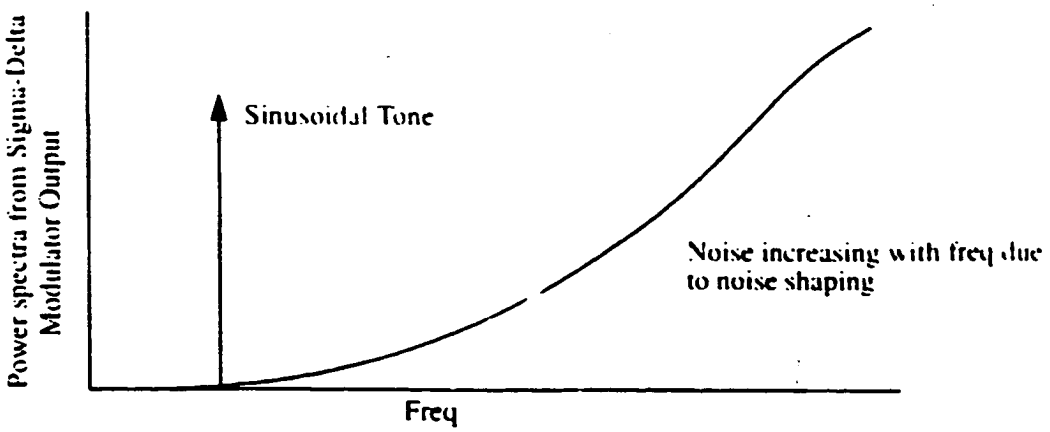


FIGURE 4.5 Spectrum from Sigma-Delta Modulation

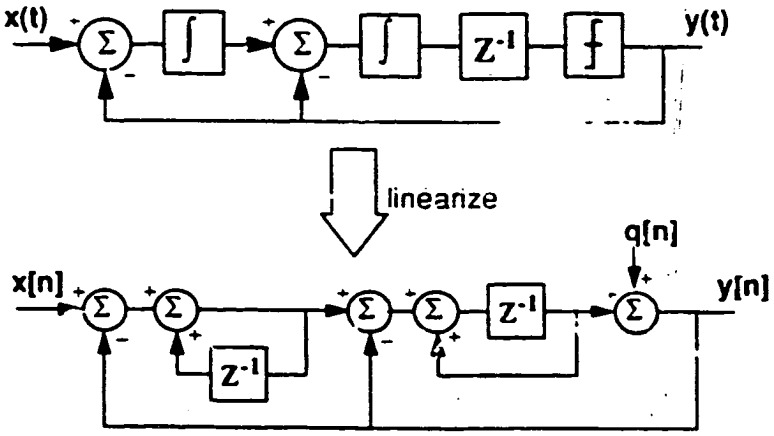


FIGURE 4.6 Double-integrating Sigma-Delta modulator

point values, increased complexity and doubling the sampling rate compared to double-integrating ΣΔ modulator (to be discussed later).

Using Multi-bit quantizers in place of the single-bit quantizer [80, 82] is another method for improving the noise shaping abilities of a ΣΔ modulator. This was shown in [45] to improve both the accuracy and stability of the ADC but relies on the linearity of the N-bit DAC in the feedback loop (N-bits as the quantizer is also N-bits) which requires again tight tolerances on components. A method to compensate for the non-linearity of the multi-bit DAC digitally was presented in [46] resulting in increased digital complexity not only for the multi-bit quantizer and DAC but also for the self-calibration procedure that must be performed. Another multi-bit quantizer architecture was introduced in [47] and eliminates the necessity for the N-bit DAC but does this by matching transfer functions in the digital side which again leads to complexity as in the MASH modulator that degrades performance.

The most common ΣΔ modulator is the double-integrating architecture shown in figure 4.6 which consists of an integrating block in front of a first-order ΣΔ modulator with negative feedback around this. Higher-order modulators can be created by nesting in the same manner more integrating blocks and feedback around this second-order ΣΔ modulator.

By replacing the quantizer in figure 4.6 by the same linearized model as in section 4.2.2, the STF is

$$STF(z) = \frac{Y(z)}{X(z)} = z^{-1}. \qquad \text{(EQ 4.4)}$$

which is the same as that for the first-order ΣΔ modulator but the NTF is different

$$NTF(z) = \frac{Y(z)}{Q(z)} = (1 - z^{-1})^2. \qquad \text{(EQ 4.5)}$$

Note that for the higher-order (Nth order) ΣΔ modulator the STF again is identical to that of a first-order but the NTF becomes

$$NTF(z) = \frac{Y(z)}{Q(z)} = (1 - z^{-1})^N \qquad \text{(EQ 4.6)}$$

Conversion from the z-domain to the frequency domain illustrates how the NTF is more attenuating to the quantization noise at low-frequencies with increasing order N

$$|NTF(f)|^2 = |NTF(z)|^2\Big|_{z = e^{j2\pi f/f_{os}}} = 4^N \sin^{2N}\left(\frac{\pi f}{f_{os}}\right) \approx 4^N \left(\frac{\pi f}{f_{os}}\right)^{2N}, (f \ll f_{os}). \qquad \text{(EQ 4.7)}$$

From the linearized equation of the NTF, it can be seen that the output quantization noise at baseband is greatly attenuated improving the SNR for a narrow baseband signal however equation 4.7 also shows that the out-of-band noise has increased considerably. Therefore in order to recover the baseband signal while preserving the SNR, the decimation filter after the modulator must become more attenuating with increasing N resulting in more complex filters.

Using the NTF, the in-band noise power can be estimated. The band of interest is defined here to be from 0 to $f_{os}/2R$ where R is referred to as the over-sampling ratio (the ratio between f_{os} and the Nyquist rate). Thus the noise power for this linearized model of the ΣΔ modulator is given by the integral

$$N_n^2 = \int_{-f_{os}/2R}^{f_{os}/2R} \sigma_n^2(f) \cdot |NTF(f)|^2 df. \qquad \text{(EQ 4.}$$

where $\sigma_n^2(f)$ is the spectral density of the quantization noise. In the discrete-time domain the sampled noise q[n] is assumed to random and uncorrelated which has been established in section 4.2.2 as valid. The quantizer is also assumed to have an input range of -1 to 1 and a discrete quantized output range of -1 or 1 and therefore q[n], the error between the input and output will range from -1 to 1 if the input range of the quantizer is not exceeded.

The autocorrelation can be easily deduced to be

$$R_q[\tau] = \begin{cases} \frac{1}{3} & \text{for } \tau = 0 \\ 0 & \text{elsewhere} \end{cases} \qquad \text{(EQ 4.9)}$$

and therefore the Z-transform of $R_q[n]$ is $\sigma_n^2(z) = 1/3$ and thus

$$\sigma_n^2(f) = T_{os} \cdot \sigma_n^2(z)\Big|_{z = e^{j2\pi f T_{os}}} = \frac{1}{3f_{os}}. \qquad \text{(EQ 4.10)}$$

Substituting back into the equation for N_0^2 gives

$$N_0^2 \equiv \frac{1}{3f_{os}} \cdot \int_{-f_{os}/2R}^{f_{os}/2R} 4^N \left(\frac{\pi f}{f_{os}}\right)^{2N} df \Bigg|_{N=2}$$
$$\equiv \frac{\pi^{2N}}{3(2N+1)R^{2N+1}}\Bigg|_{N=2} = \frac{\pi^4}{15R^5}. \qquad \text{(EQ 4.11)}$$

If now the input is assumed to be a sinusoid of amplitude A then the SNR can be estimated to be

$$SNR \equiv 10\log \frac{A^2/2}{\left(\frac{\pi^{2N}}{3(2N+1)R^{2N+1}}\right)}\Bigg|_{N=2} \text{ dB}$$
$$\equiv 10\log \frac{3A^2(2N+1)R^{2N+1}}{2\pi^{2N}}\Bigg|_{N=2} = 10\log \frac{15A^2R^5}{2\pi^4}\text{dB}. \qquad \text{(EQ 4.12)}$$

This shows that the in-band SNR for this 2nd-order modulator doubling the over-sampling ratio R increases the SNR by $10\log(2^5) = 15$ dB i.e 15 dB per octave, and for higher-orders, the SNR increases at a higher rate (6N+3 dB per octave).

The above solution is only an estimate of the performance of the ΣΔ modulator and more accurate simulations that model the quantizer appropriately as a non-linear element are re-

quired. For instance the effect of increasing the amplitude of the sine wave will at one point decrease the in band SNR because of the over-loading of the quantizer. This was demonstrated by Candy [48] and is due to feedback increasing signal levels at the input of the quantizer outside the assumed range of -1 to 1. Since the quantizer output level is either 1 or -1, the error between the quantizer output and its input can become rather large effectively increasing the noise floor. The noise produced by modulating a DC signal was also shown by Candy to be much reduced from a first-order system due to the de-correlating effects of more than 1 feedback loop.

The stability of using higher-order systems is also not evident in the SNR estimate that suggests simply that increasing N results in a higher SNR. In practice, the use of modulators with orders greater than 2 with a similar serial architecture as in figure 4.6 causes the signal levels in the integrators to become too large and the system begins to oscillate as these error signals become self-sustaining. This causes stricter tolerances on the gains of the feedback loops to ensure stability but even this is not sufficient to guarantee stability ([48]).

4.2.4 Band-Pass Sigma-Delta Modulation

The previous discussions on ΣΔ modulators has been confined to low-pass modulators that involve sampling a signal at baseband. This is because the NTF is most attenuating to the quantization noise at baseband and high-pass in nature (the STF actually places no restriction on the signal as it is all-pass). If a low-pass modulator was required to convert a band-pass signal of bandwidth f_{os}/P (keeping the same notation as the previous section) centred arbitrarily at $f_{os}/4$ at its input, then in order to preserve the SNR, the stop-band of the high-pass NTF would have to cover upto $f_{os}/4 + f_{os}/2R$. Now, previously this signal had an over-sampling ratio of R as the stop-band cut-off frequency was at $f_{os}/2R$ but now is $= f_{os}/4 + f_{os}/2R$ and therefore the over-sampling ratio is now < 2. This clearly indicates that the input to a low-pass modulator must be narrow-band and centred at 0 Hz.

In order to modify a low-pass modulator to a band-pass modulator, the NTF must be altered from being high-pass in nature to being notch-like with the notch occurring at the centre of the input signal band, thus the noise will be attenuated most around the band-of interest as it was in the low-pass case. Thus the oversampling ratio will again depend on the bandwidth of the signal and not on its centre frequency. An immediate consequence of band-pass modulators that is worth pointing out at this stage is that for the same noise shaping performance as that of a low-pass Nth-order modulator, a 2Nth-order band-pass modulator is required and this should not be surprising as this is typical of conversion between low-pass filters to band-pass filters.

One approach to designing band-pass ΣΔ modulators (BPΣΔM) is to substitute z with $-z^{-2}$ in the low-pass modulator's z-transfer functions. This was done by Longo et al. [49] to transform the double-integrating ΣΔ modulator in section 4.2.3 into its band-pass equivalent. This resulted in the following NTF

$$NTF(z) = (1 - w^{-1})^2 \Big|_{w = -z^{-2}} = (1 + z^{-2})^2 \qquad \text{(EQ 4.13)}$$

which has zeroes located a z = j and -j, both with a multiplicity of 2. Note this is similar to the low-pass case which has zeroes at z = 1 with multiplicity of 2. The locations of the zeroes of the NTF implies that the notch of the NTF is located at f_{OV} and therefore the narrowband input signal would have to have its frequency band centred there. Using the same derivations as the previous section except substituting the fact that a Nth-order BPΣΔM has the same noise shaping characteristics as a (N/2)th-order low-pass modulator, the SNR can be shown to increase at 3N + 3 per octave of R.

The STF becomes

$$STF(z) = z^{-2} \qquad \text{(EQ 4.14)}$$

which again has an all-pass characteristic.

A more general approach is to use architectures with enough coefficients in the transfer function so as to be able to place the poles and zeroes at the desired locations similar to that in designing digital filters [55] where optimization for stability can then take place. The effects of limiting at the integrators can also be eliminated or reduced by careful selection of integrator time constants and coefficients. A similar approach is the cascade-of-resonator architecture [51, 85] that again allows for not only the customization of the NTF but also of the STF. One obvious advantage to this it that the STF can be made band-pass as opposed to the typical all-pass. Jantzi et al. [50, 83] used this approach to designing their BPΣΔM and it its this approach that will be used in the subsequent sections to design the BPΣΔM that is to be used in the DECT receiver.

4.3 A BANDPASS SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER FOR DECT

The purpose of the bandpass sigma-delta ADC (BPΣΔADC) in this DECT receiver architecture is to sub-sample the DECT RF signal that has already been down-converted by a mixer to its IF (about 100 MHz). This conversion process will digitally down-convert the IF signal to baseband while also splitting the baseband information into its in-phase and quadrature components so that quadrature demodulation can then be performed.

The BPΣΔADC performs this task in the following manner: the IF signal is sub-sampled using the BPΣΔM and its 1 bit output is multiplied by an in-phase and quadrature sine wave to down-convert to baseband into its in-phase and quadrature components. These 2 signals are then decimated to the required analog-to-digital conversion rate and because the decimation process also involves removal of the quantization noise from ΣΔ modulation, the baseband signal is recovered with a high SNR and the digital output now has multi-bit resolution.

4.3.1 System Requirements

First the final baseband conversion rate must be determined as well as the required baseband processing bit resolution which are both dependent upon the method of demodulation and bit synchronization (timing recovery). For this receiver, the demodulator presented in [37] was chosen because of its detailed direct application to DECT. Its bit timing is recovered by deciding which sample out of the 8 samples that are taken in a bit period has the largest eye-opening and then using that sample to recover the bit information. Thus the conversion rate of the ADC is 9.216 Msamples/s, 8 times that of the 1.152 Mbps transmission bit rate of DECT. The bit resolution is determined by the ability of the demodulator to extract the signal from the receiver's noise floor and is characterized by the SNR needed for a certain BER. For the demodulator chosen, a SNR of 14 dB was required to obtain a BER of 10^{-3} (a BER of 10^{-3} is used in the ETSI DECT standard [10] as the measure of sensitivity level) which was shown in [37] to be comparably to the theoretical performance of non-coherent FSK of 11 dB when the increase in noise bandwidth was included for frequency offset and bit timing recovery inaccuracy of upto 1/16th of a bit period was factored in. This implies that the noise floor of the receiver system including the quantization noise from the finite bit resolution after analog-to-digital conversion must be lower than the signal level received by at least 14 dB in order for the BER to be better than 10^{-3}. In chapter 2, the noise floor of the system after digitization was computed when the received signal was weakest which is where the SNR would be the most critical, and the theoretical minimum bit resolution for 14 dB SNR was found to be 3. However, a 6-bit ADC is necessary so that the quantization noise introduced would not greatly impact the residual BER of the demodulator. The SNR level designed for in the BP$\Sigma\Delta$M will be 48 dB. This extra margin is necessary as quantization from truncations/rounding in the digital signal processing and other circuit non-idealities will add to the overall noise.

The next step is to determine the OSR from the SNR requirement of 48 dB (see chapter 2 for conversion of bit resolution to SNR). It is demonstrated below that the OSR chosen is

dependent upon the order of the modulator where in general, a smaller OSR can be obtained for the same SNR using a higher order modulator but, as in the low-pass case the "cost" of using a higher order modulator is an increase in complexity and instability.

Schreier and Snelgrove in [38] derived an expression for the SNR of a BPΣΔM which had all its zeroes at a specific frequency by assuming that near a zero of order N, the magnitude of the NTF can be approximated by

$$|NTF(e^{jw})| = k(w - w_0)^N \qquad \text{where } k = \frac{1}{N!}\frac{d^N}{dw^N}|NTF(e^{jw})|\Big|_{w = w_0} \qquad \text{(EQ 4.15)}$$

and therefore the SNR can be derived as in the low-pass case to be

$$SNR \cong 10\log\left(\frac{3A^2(N+1)(2R)^{N+1}}{4k^2\pi^N}\right) \text{ dB.} \qquad \text{(EQ 4.16)}$$

The values for k from [50] and [38] are k = 1.414 for N = 2, k = 13 for N = 13 and k = 8.6 for N = 6 and applying these into the equation for SNR gives the estimated over-sampling ratio, R for each order N that produces 48 dB SNR (see table 4.1). The estimates suggests that the minimum order BPΣΔM that will provide the necessary in-band SNR without sampling at an extremely high rate is N = 6. This still has to be verified with simulations using a customized NTF.

Now that the order of the modulator has been established using linear approximations, a Z-domain linear model can be developed to optimize the NTF and STF for good SNR performance and signal bandpass performance while maintaining stability followed by further verification with simulations using a non-linear model.

4.3.2 Cascade-of-Resonator Architecture

The Cascade-of-Resonator structure was used first in [51] to implement a low-pass ΣΔ modulator and was subsequently applied in [50] to implement a BPΣΔM. This architecture

was optimized to be used with switched capacitor building blocks and circuit techniques and therefore its many advantages are based upon this. There has been already examples of low-pass ΣΔ modulators with over-sampling rates of 50 MHz [52, 53] using 1 and 1.2μm CMOS technology switched-capacitor circuit techniques, and with sub-micron CMOS and BiCMOS technologies becoming available, higher sampling rates of upto 200 MHz are now possible [54] and one expects that these circuit techniques will remain dominant even for the more complex BPΣΔM.

The advantages of the Cascade-of-resonator architecture [51] (see figure 4.7) is that the feedback is distributed to several summation nodes enhancing the stability of the system and thus worst case settling occurs with 2 amplifiers in series. And unlike the other multi-order loop structures [55, 56] which allow for pole and zero placement, this distributed structure also does not require multiple coefficient summers at the input and output. The basic building block is an integrator which is easily implemented using switched-capacitor techniques and an op-amp. The placement of 2 of these integrator blocks together with 2 delay elements results in a resonator (hence the architecture's name).

The linear Z-domain representation of a sixth-order cascade-of-resonator ΣΔ modulator is shown in figure 4.7. This is similar to that used in [50] except an extra coefficient is added to the feed-forward branches to provide 6 zeroes in the STF to improve its out-of-band attenuation abilities as compared to [50] with minimal increase in complexity (the linear NTF is identical).

4.3.3 The Noise Transfer Function

The NTF can be derived by setting x[n] = 0 for all n therefore the coefficients a_i have no contribution to the NTF equation (see figure 4.8)

Let G = 1/(z-1) therefore in the complex Z-domain

$$E_1 = -h_{11}Y - zR_1E_2G, \qquad \text{(NTF1)}$$

N	2	4	6
k	1.414	13	8.6
R	191	62	19
f_{os} [MHz]	660	214	65

TABLE 4.1 Over-sampling Rate for 48 dB SNR

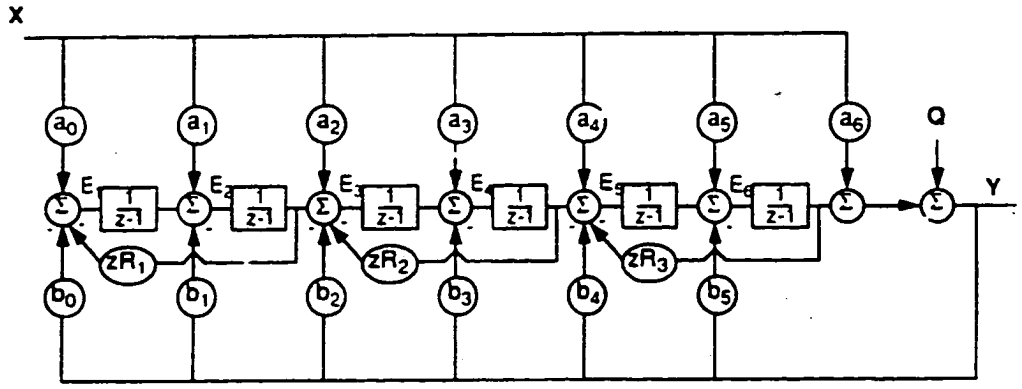


FIGURE 4.7 Linear Z-domain representation of Cascade-of-resonator ΣΔ modulator (N=6)

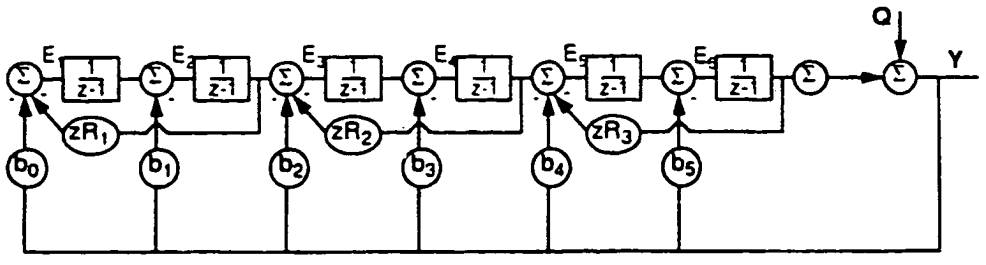


FIGURE 4.8 Equivalent (linear) Noise Transfer function representation

$$E_2 = E_1 G - h_2 Y. \qquad \text{(NTF2)}$$

$$E_3 = -h_2 Y - zR_2 E_4 G + E_2 G. \qquad \text{(NTF3)}$$

$$E_4 = E_3 G - h_3 Y. \qquad \text{(NTF4)}$$

$$E_5 = -h_4 Y - zR_3 E_6 G + E_4 G. \qquad \text{(NTF5)}$$

$$E_6 = E_5 G - h_5 Y. \qquad \text{(NTF6)}$$

$$Y = E_6 G - Q. \qquad \text{(NTF7)}$$

Now combining NTF1 with NTF2 gives

$$E_2 = -h_0 YG - zR_1 E_2 G^2 - h_1 Y$$

$$\Rightarrow E_2 = \frac{-(h_1 + h_0 G)\, Y}{(1 + zR_1 G^2)}. \qquad \text{(NTF8)}$$

Substituting into NTF3

$$E_3 = -h_2 Y - zR_2 E_4 G + \frac{-(h_1 + h_0 G)\, Y}{(1 + zR_1 G^2)} \qquad \text{(NTF9)}$$

and continuing along in the same manner, the NTF = Y(z)/Q(z) has a numerator equal to

$$num\,(NTF) = 1 + z\,(R_1 + R_2 + R_3)\,G^2 + [z^2 R_1 R_2 + z^2\,(R_1 + R_2)\,R_3]\,G^4 + z^3 R_1 R_2 R_3 G^6$$

and a denominator equal to

$$\begin{aligned} den(NTF) = {} & 1 + b_5 G + [z(R_1 + R_2 + R_3) + b_4] G^2 \\ & + [b_3 + z(R_1 + R_2) b_5] G^3 \\ & + [b_2 + z(R_1 + R_2) b_4 + z^2 R_1 R_2 + z^2 (R_1 + R_2) R_3] G^4 \\ & + [b_1 + z R_1 b_3 + z^2 R_1 R_2 b_5] G^5 \\ & + [b_0 + z R_1 b_2 + z^2 R_1 R_2 b_4 + z^3 R_1 R_2 R_3] G^6. \end{aligned}$$

Next the denominator is multiplied by $1/G^6$ and expanded to obtain the coefficients for each power of z

z^6: 1.

z^5: $-6 + b_5 + (R_1 + R_2 + R_3)$.

z^4: $15 + b_5(R_1 + R_2 - 5) + b_4 - 4(R_1 + R_2 + R_3) + (R_1R_2 + R_1R_3 + R_2R_3)$.

z^3: $R_1R_2R_3 - 20 + b_5(10 - 3(R_1 + R_2) + R_1R_2) + b_4(R_1 + R_2 - 4) + b_3$
$+ 6(R_1 + R_2 + R_3) - 2(R_1R_2 + R_1R_3 + R_2R_3)$.

z^2: $b_5(3(R_1 + R_2) - 10 - R_1R_2) + b_4(R_1R_2 + 6 - 2(R_1 + R_2)) + b_3(R_1 - 3)$
$+ b_2 - 4(R_1+R_2+R_3) + (R_1R_2+R_1R_3+R_2R_3) + 15$.

z: $b_5(5 - (R_1 + R_2)) + b_4(R_1 + R_2 - 4) + b_3(3 - R_1) + (R_1 - 2)b_2 + b_1$
$+ (R_1 + R_2 + R_3) - 6$.

1: $-b_5 + b_4 - b_3 + b_2 - b_1 + b_0 + 1$.

A similar analysis for the numerator num(NTF) results in the following coefficients for each power of z in the numerator polynomial

z^6: 1.

z^5: $(R_1 + R_2 + R_3) - 6$.

z^4: $15 - 4(R_1 + R_2 + R_3) + (R_1R_2 + R_1R_3 + R_2R_3)$.

z^3: $R_1R_2R_3 - 20 + 6(R_1 + R_2 + R_3) - 2(R_1R_2 + R_1R_3 + R_2R_3)$.

z^2: $15 - 4(R_1 + R_2 + R_3) + (R_1R_2 + R_1R_3 + R_2R_3)$.

z: $(R_1 + R_2 + R_3) - 6$.

1: 1.

Note that the coefficients in the numerator polynomial are symmetrical and that it is equivalent to the denominator coefficients with all the parameters b_i set to zero. Also the numerator polynomial is governed by the coefficients R_1, R_2 and R_3 whereas the denominator is characterized by both coefficients b_i and R_j.

4.3.4 Signal Transfer Function

Using the same method of analysis as above the STF can be derived by setting the quantization noise q[n] = 0 (Q(z) = 0). Thus at each node E_i in figure 4.7 the following equations hold:

$$E_1 = a_0X - b_0Y - zR_1E_2G. \qquad \text{(STF1)}$$

$$E_2 = a_1X + E_1G - b_1Y. \qquad \text{(STF2)}$$

$$E_3 = a_2X - b_2Y - zR_2E_4G + E_2G. \qquad \text{(STF3)}$$

$$E_4 = a_3X + E_3G - b_3Y. \qquad \text{(STF4)}$$

$$E_5 = a_4X - b_4Y - zR_3E_6G + E_4G. \qquad \text{(STF5)}$$

$$E_6 = a_5X + E_5G - b_5Y. \qquad \text{(STF6)}$$

$$Y = E_6G + a_6X. \qquad \text{(STF7)}$$

Using STF7 and solving for E_6

$$E_6 = \frac{Y - a_6X}{G} \qquad \text{(STF8)}$$

and substituting back into STF6 and then solving for E_5 gives

$$E_5 = (a_4 + a_6 zR_3)X - (b_4 + zR_3)Y + E_4 G.$$

Continuing along with this process finally results in the STF = Y(z)/X(z) where the numerator of STF = num(STF) is given by

$$\begin{aligned} num(STF) &= a_0 + a_5 + [z(R_1 + R_2 + R_3)a_6 + a_4]G^2 \\ &\quad + [z(R_1 + R_2)a_5 + a_3]G^3 \\ &\quad + [z^2(R_1R_2 + R_1R_3 + R_2R_3)a_6 + z(R_1 + R_2)a_4 + a_2]G^4 \\ &\quad + [z^2R_1R_2a_5 + zR_1a_3 + a_1]G^5 \\ &\quad + [z^3R_1R_2R_3a_6 + z^2R_1R_2a_4 + zR_1a_2 + a_0]G^6 \end{aligned}$$

and the denominator of STF = den(STF)

$$\begin{aligned} den(NTF) &= 1 + b_5G + [z(R_1 + R_2 + R_3) + b_4]G^2 \\ &\quad + [b_3 + z(R_1 + R_2)b_5]G^3 \\ &\quad + [b_2 + z(R_1 + R_2)b_4 + z^2R_1R_2 + z^2(R_1 + R_2)R_3]G^4 \\ &\quad + [b_1 + zR_1b_3 + z^2R_1R_2b_5]G^5 \\ &\quad + [b_0 + zR_1b_2 + z^2R_1R_2b_4 + z^3R_1R_2R_3]G^6. \end{aligned}$$

Notice that the denominator of both the NTF and the STF are the same i.e. den(NTF) = den(STF). Thus the coefficients of each power of z in the denominator polynomial is the same as that derived in the previous section.

The numerator num(STF) polynomial coefficients can be derived by expanding the expression obtained by multiplying num(STF) with $1/G^6$ and results in the following

z^6: a_6.

z^5: $[(R_1 + R_2 + R_3) - 6]a_6 + a_5$.

z^4: $[15 - 4(R_1 + R_2 + R_3) + (R_1R_2 + R_1R_3 + R_2R_3)]a_6 + (R_1 + R_2 - 5)a_5$

$+ a_4$.

z^3: $[R_1R_2R_3 - 2(R_1R_2 + R_1R_3 + R_2R_3) + 6(R_1 + R_2 + R_3) - 20]a_6$
$+ (10 - 3(R_1 + R_2) + R_1R_2)a_5 + (R_1 + R_2 - 4)a_4 + a_3$.

z^2: $[15 - 4(R_1+R_2+R_3) + (R_1R_2+R_1R_3+R_2R_3)]a_6$
$+ [3(R_1 + R_2) - 10 - R_1R_2]a_5 + [6 - 2(R_1 + R_2) + R_1R_2]a_4$
$+ (R_1 - 3)a_3 + a_2$.

z: $[(R_1 + R_2 + R_3) - 6]a_6 + [5 - (R_1 + R_2)]a_5 + (R_1 + R_2 - 4)a_4$
$+ (3 - R_1)a_3 + (R_1 - 2)a_2 + a_1$.

1: $a_6 - a_5 + a_4 - a_3 + a_2 - a_1 + a_0$.

The numerator of STF is characterized by both coefficients a_i and R_j whereas as mentioned before in the previous section the denominator (which is common to both STF and NTF) is established by both coefficients b_i and R_j.

4.3.5 Optimization of the Noise Transfer Function

The dependence between the transfer functions (STF and NTF) and the coefficients a_i, b_i and R_j has now been established and also shows that the denominator and therefore pole locations of denominator polynomial for both functions are the same. The next step is to optimize the performance of the BPΣΔM for rejection of the quantization noise for the band-of-interest specific to this receiver architecture (around $f_{os}/4$ of the modulator while maintaining stability by pole/zero placement of the NTF and customizing the STF to some degree by placement of the zeroes in the STF (its pole locations has already been determined as it has the same poles as the NTF.

The pole and zero locations of the NTF are constrained by the requirement that the NTF must be extremely attenuating at $f_{os}/4$ while maintaining stability. One measure of noise rejection of an NTF, that is used here, is integrating the squared magnitude of the NTF within the band of interest. Thus better attenuation can be achieved by minimizing this measure. A general stability criterion for non-linear ΣΔM systems has yet to be developed

that would predict instability accurately, however more traditional digital filter theory can be used with the linearized model of the modulator and suggest that for stability, the z-domain poles be placed within the unit circle ($|z| < 1$). Unfortunately, this does not take into account the limited range of the quantizer which is a non-linear mechanism for instability. Previously, the quantization noise was derived in section 4.2.3 assuming that the normalized range of the quantizer is from -1 to 1 and is never exceeded. If the signal input into the quantizer is outside this range, the resulting quantization noise at the output becomes greater and when feedback into the system, can cause an even greater signal to appear again at the input to the quantizer and gradually the dynamic range of the system is swallowed by the noise resulting in instability and the output becomes non-informative. Lee [57] deduced that this places a constraint on the magnitude of the NTF to be less than 2. However this condition was found to be both unnecessary and insufficient but also stated that if used with margin, results often in a stable system [58].

To summarize, the constraints on the NTF are:

(a) maximize in-band SNR by minimizing

$$\int_{\omega_0 - \pi/2R}^{\omega_0 + \pi/2R} |NTF(z)|^2 d\omega \Big|_{z = e^{j\omega}}$$

where $\omega_0 = \pi/2$ is the centre of the band-of-interest ($\omega_0 - \pi/2R$, $\omega_0 + \pi/2R$) and R is the OSR.

(b) NTF(ω = infinity) = 1 (for realizability).

(c) Z-domain poles of NTF must be within unit circle. Actual condition used is $|z_{pole}| < 0.96$ to provide enough margin such that any variation in coefficients does not place the poles outside the unit circle.

(d) |NTF| < 1.6 at out-of-band frequency (includes margin on Lee's proposed |NTF| < 2

(e) Both poles and zeroes occur in conjugate pairs as this forces the polynomial coefficients and therefore a_i, b_i and R_j to be real valued. Thus in terms of pole/zero location, only 3 poles and 3 zeroes are placed as the other three are automatically located as the complex conjugate. They were also placed symmetrically about imaginary z-axis such that the bandpass frequency response would be symmetrical about $\omega = \pi/2$.

The optimization was performed using Matlab with the following initial conditions:

(i) R = 18. This was chosen to be one less than the value of 19 predicted in section 4.3.1 as it forces the band-of-interest to be slightly wider.

(ii) The initial values of the zeroes of the NTF are

$$z_{zero} = j \text{ for all zeroes.}$$

This places all the zeroes at the centre of the band-of-interest initially and the optimization should spread these zeroes out across the band if it proves to be more beneficial.

(iii) The poles are placed rather arbitrarily close to the zeroes within the unit circle as to comply with both constraints (c) and (d)

$$z_{p1} = 0.0363 +/- 0.6926j,$$

$$z_{p2} = 0.1754 +/- 0.9371j,$$

$$z_{p3} = -0.1856 +/- 0.9203j.$$

The optimization resulted in the following pole/zero locations:

$$z_{z1} = +/- j,$$

$$z_{z2} = 0.0683 +/- 0.9977 j,$$

z_{z3} = -0.0683 +/- 0.9977 j.

z_{p1} = +/- 0.6893 j.

z_{p2} = 0.2066 +/- 0.9102 j.

z_{p3} = -0.2066 +/- 0.9102 j.

The effects of spreading the zeroes out in the band-of-interest on the NTF is illustrated in figure 4.9. The in-band noise power was found to have decreased by 8 dB by placing the poles in a more optimal position than just at z = +/- j.

4.3.6 Optimization of the Signal Transfer Function

The denominator of the STF is the same as that of the NTF which has already been determined in the previous section. The remaining parameters to be valued are the location of the zeroes of the STF. There are 3 complex conjugate pairs and that limits the customization of the shape of the STF. The basic requirements of the STF should be a balance between the bandpass response around the band-of-interest with reasonable stop-band rejection while maintaining minimal distortion of the desired DECT channel at $f_{os}/4$.

Thus the following constraints are used to derive the STF:

(a) Flat passband response i.e. minimize amplitude deviation from centre frequency.

$$min\{|STF(\omega)| - |STF(\omega_o)|\}$$

where ω is in the passband ($\omega_0 - \pi/2R$, $\omega_0 + \pi/2R$), R = 18 and $\omega_0 = \pi/2$.

(b) attenuation in stop-band > 10 dB. This value was selected somewhat arbitrarily as the main emphasis is to make the passband maximally flat and 10 dB stop-band attenuation did not seem to restricting from experimentation.

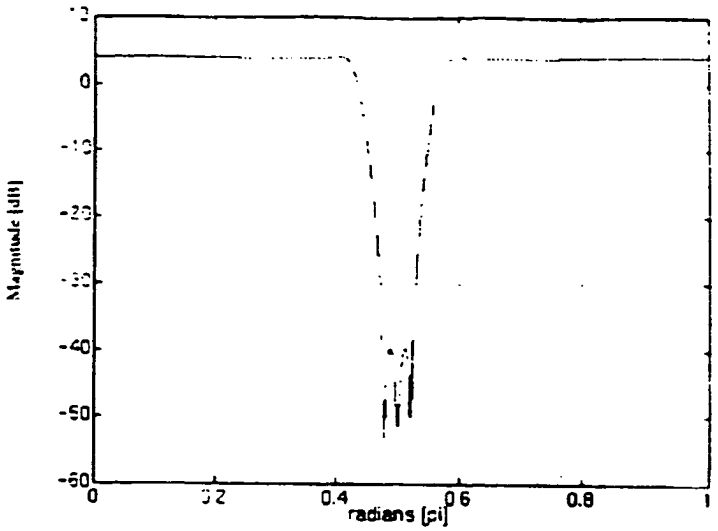


FIGURE 4.9 Optimized Noise Transfer function frequency response

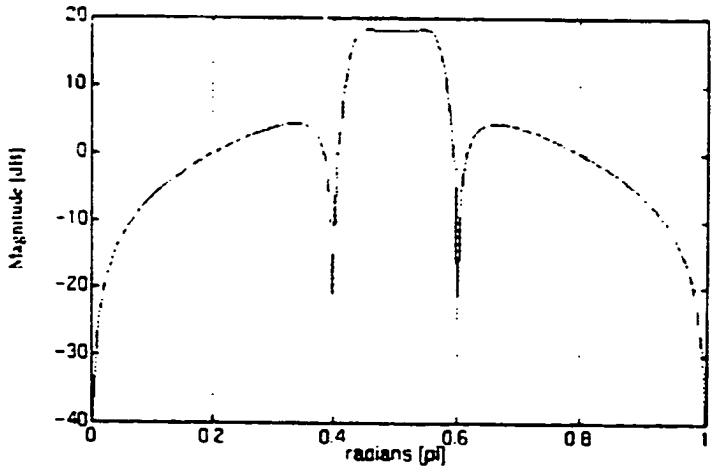


FIGURE 4.10 Optimized Signal Transfer function frequency response

(c) the zeroes are constrained to be in complex conjugate pairs to ensure that the polynomial coefficients of the numerator of the STF are real. They are also located on the unit circle and symmetrically about the imaginary z-axis such that the bandpass response would be symmetrical.

(d) one conjugate pair of zeroes was placed at z = 1 and z = -1. This places a notch in the STF at multiples of $f_{os}/2$ and is used to reject any spurious from the harmonics of the 1.152 MHz DECT symbol rate that may occur on the printed circuit board.

Thus only one angle is required to determine the location of the remaining two conjugate pair of poles. Optimizing again using Matlab results in the following zero locations:

$$z_{z1} = 0.314 +/- 0.949\ j.$$
$$z_{z2} = -0.314 +/- 0.949\ j.$$

The STF is shown in figure 4.10.

4.3.7 Simulation of the Bandpass Sigma-Delta Modulator

The previous analysis provides only an estimate of the modulator performance, therefore a simulation of the modulator is still required to see if the response is as predicted and stable. Using the pole and zero of the NTF and STF found in section 4.3.5 and section 4.3.6 the coefficients a_i, b_i and R_j of the cascade-of-resonator structure in figure 4.7 was deduced in Appendix C using the relationships derived in section 4.3.3 and section 4.3.4. A discrete-time domain simulation of the modulator including the non-linear 1-bit quantizer was then performed with Matlab. The quantizer was modeled as a hard decision element whose output was 1 if its input was greater than zero otherwise its output was -1. A sinusoid at a frequency of 1/4 the sampling rate (of the modulator, f_{os}) was used as the test input signal and had an amplitude 10 dB lower than the quantizer range i.e 0.316 so as not to

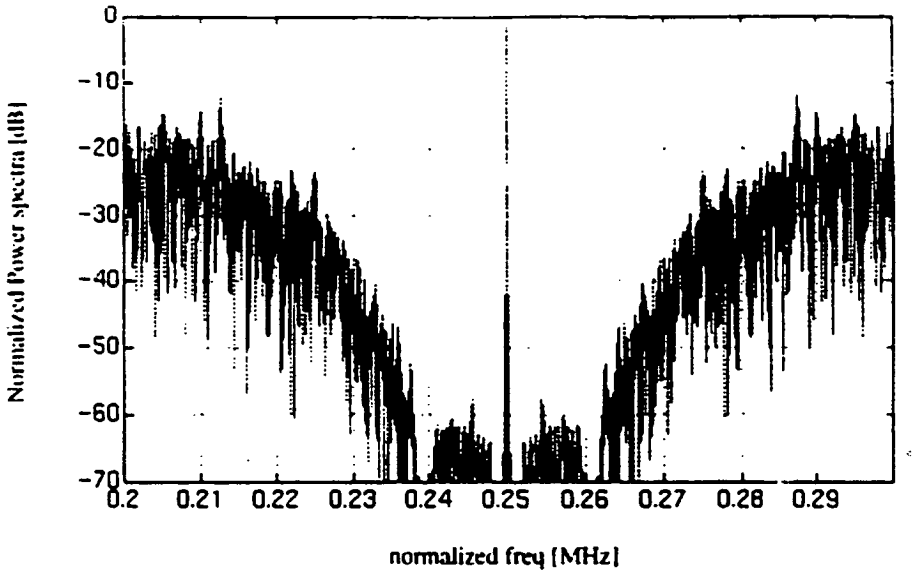


FIGURE 4.11 Output spectrum of BPΣΔM with a sinusoidal input

saturate and overload the modulator. The FFT of the output was then computed and plotted (see figure 4.11).

The results confirms that the design is indeed stable and that the in-band quantization noise of the modulator is flat and not a notch. For the desired 48 dB SNR and from figure 4.11, the bandwidth where the SNR is indeed greater than 48 dB (BW_{SNR}) is 0.08π rad/s = $0.08(f_{os}/2) = 0.04f_{os}$.

4.3.8 Over-Sampling Frequency

Now that the relationship between the in-band bandwidth (BW_{SNR}) and the over-sampling rate of the modulator, f_{os} has been determined through simulation in the previous simulation, an actual suitable value for f_{os} can be computed with the following conditions:

(a) The bandwidth of a single DECT RF channel (BW_{DECT}) is 1.728 MHz [10] and since $BW_{DECT} < (BW_{SNR} = 0.04f_{os})$ therefore the lower limit of 43.2 MHz for f_{os} ensures that quantization noise in-band is sufficiently low.

$$f_{os} > 43.2 \text{ MHz.}$$

The upper limit of f_{os} is restricted by the technology used to build the modulator and the need for low-power consumption.

(b) f_{os} must be a multiple of the conversion rate, f_{conv} = 9.216 Mbps (see section 4.3.1) because it is a lot easier to decimate if the decimation factor is an integer.

$$f_{os} = D(B(1.152)) \text{ MHz}$$

where D is the decimation factor and B = 8 (which implies f_{conv} = 9.216 Mbps)

(c) f_{os} and f_{IF} (the IF frequency of the receiver) are related in quadrature sampling by (see section 3.5.5)

$f_{os} = 4f_{IF} / (2n + 1)$.

Thus determining the f_{os} constrains f_{IF} to a certain set of values and vice versa.

Although the DECT standard [10] does not specify any IF frequency value, manufacturers of SAW filters (e.g. TOKO, SAWTEK) have selected 110.592 MHz as the preferred value and thus DECT SAW filters with that centre frequency are commonly available. The reason for this is that the radio designer is relatively free to choose the IF frequencies in the receiver, however a custom designed SAW would be required unless one is already available at that frequency meeting the necessary specifications. In order to control costs, a specific IF frequency was decided upon allowing manufacturers to make SAWs in large quantities.

Thus combining the conditions of (b) and (c)

$$\frac{f_{os}}{f_{conv}} = D = \frac{4}{2n+1}\left(\frac{f_{IF}}{f_{conv}}\right) \quad \text{where D, n, B} \in Z, \qquad \text{(EQ 4.17)}$$

with the values for $f_{conv} = B(1.152)$ and $f_{IF} = 110.592$ gives

$$D = \frac{4}{(2n+1)B}\left(\frac{110.592}{1.152}\right) = \frac{384}{(2n+1)B}. \qquad \text{(EQ 4.18)}$$

Using B = 8, there are no integer values of n such that D is an integer. Actually, even if B was not confined to 8, the only set of values for {D, n, B} possible is when n = [illegible] 384 = 3(4)(4)(8). This implies that for this architecture f_{IF} cannot be 110.592 MHz. Thus a custom IF SAW would have to be constructed but this does not mean that any value for f_{IF} is possible. The centre frequency of the SAW is still constrained by SAW technology and the other commercially available ICs that are to form the IF chain of the receiver specifically the IF limiter. Since the IF limiter that is to be used (National Semiconductor LMX2240)

has already been designed to operate at about 110.592 MHz, a similar frequency would have to be chosen for f_{IF}.

This still leaves quite a few possibilities for f_{IF} when B = 8

$$f_{IF} = 2(2n + 1)(1.152)D \text{ MHz.} \qquad \text{(EQ 4.19)}$$

The lowest value of f_{IF} that satisfies the above requirements is 103.68 MHz. With B = 8, the remaining values for D and n that satisfy those 3 conditions and also results in the lowest value for f_{os} become D = 5, n = 4 and f_{os} = 46.08 MHz. However this was not chosen as this falls inside the commercial radio FM broadcast band and thus would be subject to interference from their transmissions. Another reason for its rejection is that the decimation factor is odd whereas an even number results in a notch created by the CIC response being located at $f_{os}/2$ which is where the image after quadrature separation falls (see figure 4.13). Thus next lowest f_{IF} = 124.4160 MHz was chosen (D = 6, n = 4 and f_{os} = 55.2960 MHz).

Using the sampling rate established here, the modulator was re-simulated with the input being equivalent to a GMSK signal with a frequency deviation of 288 kHz, a bandwidth-bit period product BT = 0.5, symbol-rate T = 1.152 Mbps, over-sampling rate = 55.2960 MHz and an IF frequency of 124.4160 MHz. The fast-Fourier transform of the output of the modulator is shown in figure 4.12.

4.3.9 Quadrature Separation

The digital output of the modulator is a single bit word at a rate of 55.2960 MHz containing both the desired in-band signal, centred at 1/4 the sampling rate with high SNR, and the out-of-band quantization noise. The in-phase and quadrature components must now be recovered, followed by decimation to the required 9.216 MHz baseband sampling rate and the removal of out-of-band noise.

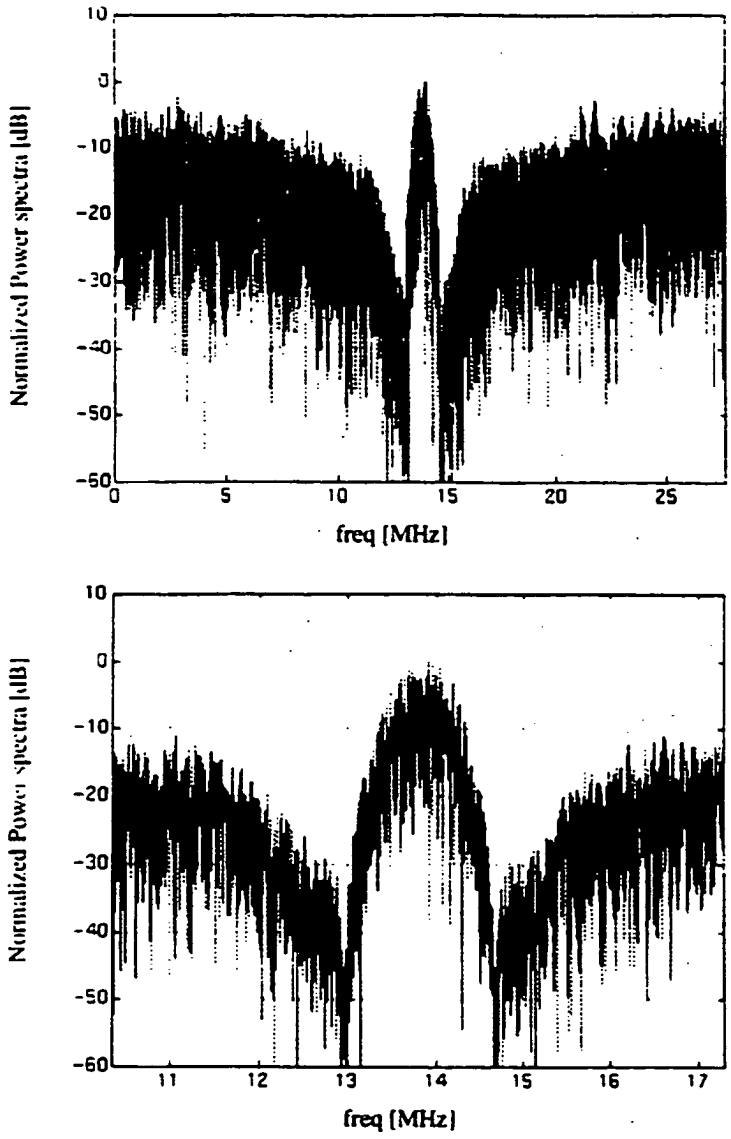


FIGURE 4.12 Output spectrum of BPΣΔM with a GMSK signal input

The first step is to separate the signal into its in-phase and quadrature baseband components by multiplying the samples by cosine and sine waves of frequency $f_{os}/4$ (13.824 MHz). Because of the proper selection of f_{IF} and f_{os} (i.e. $f_{os} = 4f_{IF}/(2n + 1)$) this is equivalent to simply multiplying the samples (which are either -1 or 1) by ... 1, 0, -1, 0, 1, ... and .... 0, 1, 0, -1, 0, ... respectively which can be easily realized by discarding every other sample to save storage space (but remembering that there are zeroes in between the samples) and also alternating the signs of the retained samples (since every other sample is zero, the effective processing rate has been halved). The in-phase or quadrature spectrum is now centred at baseband which eases the decimation process (most developments in decimation assumes that the desired signal is at baseband).

4.3.10 Cascaded Integrator-Comb Decimation

The decimation process reduces the sampling rate from $f_{os} = 55.2960$ MHz to the required $f_{conv} = 9.216$ MHz baseband sampling rate (decimation factor of 6). Because of the out-of-band quantization noise a lot of aliasing can occur during this rate reduction and therefore decimation is not as simply as just discarding every four samples for every one kept but requires a decimation filter to reduce the aliasing of the out-of-band noise that falls in-band to an acceptable level.

These aliasing bands can be found from understanding the effects of decimation on the spectrum of the signal. If a signal $X(e^{j\omega})$ is decimated by a factor D, the resultant signal spectrum is given by [59]

$$X_d(e^{j\omega}) = \frac{1}{D}\sum_{i=0}^{D-1} X\left(e^{j\left(\frac{\omega}{D} - \frac{2\pi i}{D}\right)}\right). \qquad \text{(EQ 4.20)}$$

In words, the spectrum $X(e^{j\omega})$ is expanded by the factor D (relative to the lower sampling rate) and then D of these are summed together each of them offset from the previous one by the lower sampling rate (with the first one starting with no offset). This is illustrated in

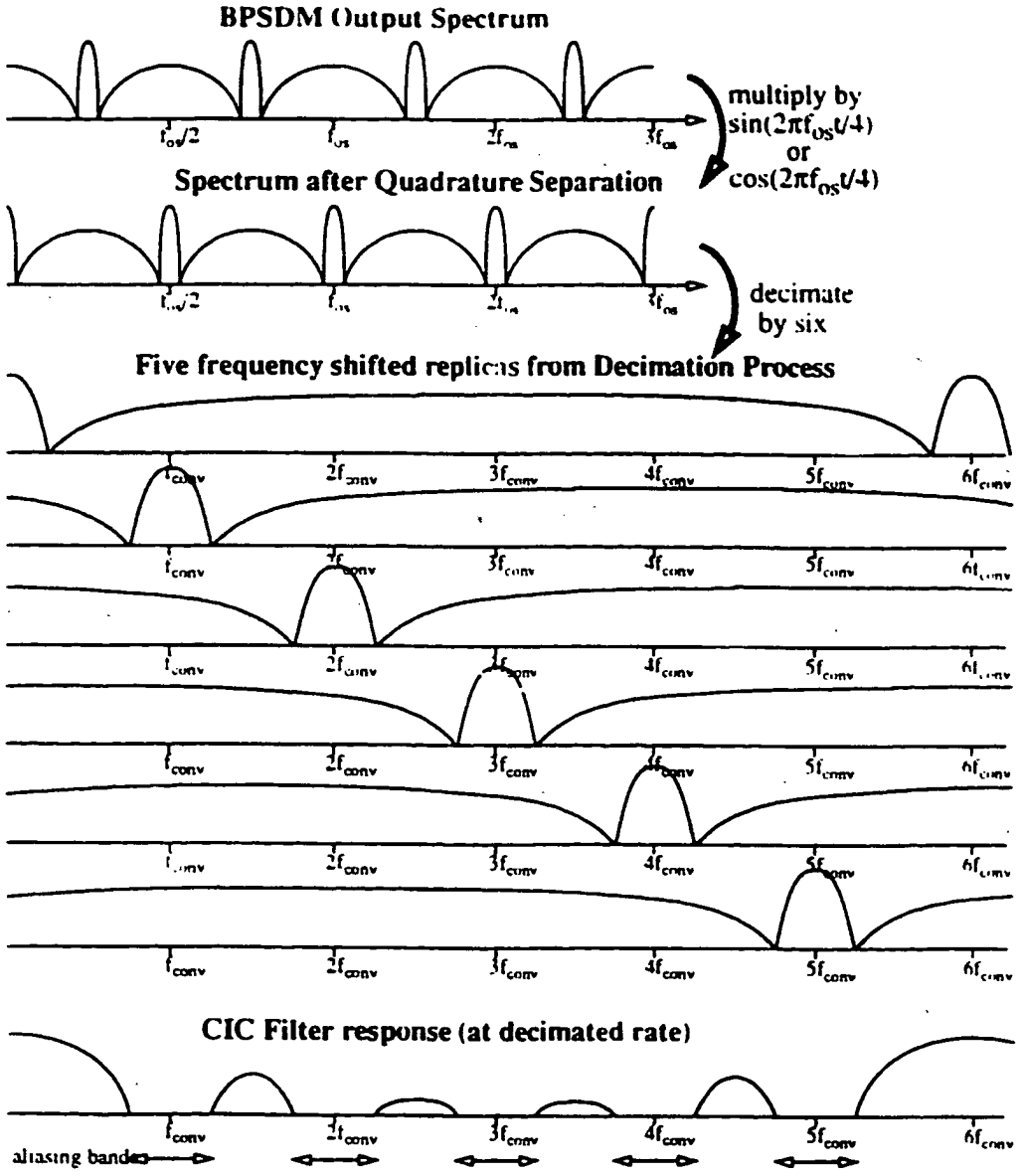


FIGURE 4.13 Decimation Process

figure 4.13 using D = 6, higher sampling rate = f_{os} and the lower rate = f_{conv}. Thus the aliasing bands occur at multiples of the lower sampling rate (f_{conv}).

The cascaded integrator-comb (CIC) filter architecture [60] is used to perform the decimation and provides a $sinc^N$ response that has zeroes at multiples of the decimated rate, f_{conv} (9.216 MHz) effectively attenuating the out-of-band noise that is aliased in-band during decimation but does not attenuate this noise throughout all the frequencies (due to high side lobes of $sinc^N$) such that the noise floor after decimation is below 48 db SNR level. This is left to filtering after the decimation process, that operates at f_{conv} and therefore makes it more economical in terms of processing power.

The CIC architecture is illustrated in figure 4.14 and was chosen because its implementation contains no multipliers (just adders), no storage of filter coefficients (because individual stages have unity coefficients), reduces the amount of storage registers by cascading integrator and comb sections together to implement the $sinc^N$(the conventional FIR method of implementing the $sinc^N$ requires much more storage registers), and has also a regular structure that can be exploited in standard cell CMOS designs.

Each integrator stage has a transfer function of

$$I(z) = \frac{1}{1 - z^{-1}} \qquad z = e^{j2\pi fT_{os}} \qquad \text{(EQ 4.21)}$$

where z is referenced to the higher sampling rate = f_{os}.

The comb stage is operating at the decimated rate $f_{ccnv} = f_{os}/D$ (where D = 6, determined from section 4.3.8) and has a transfer function

$$C(Z) = (1 - Z^{-D}) \qquad Z = e^{j2\pi fT_{conv}} \qquad \text{(EQ 4.22)}$$

where Z is referenced to the decimated rate f_{conv}. Rewriting C(Z) in terms of the higher sampling rate results in

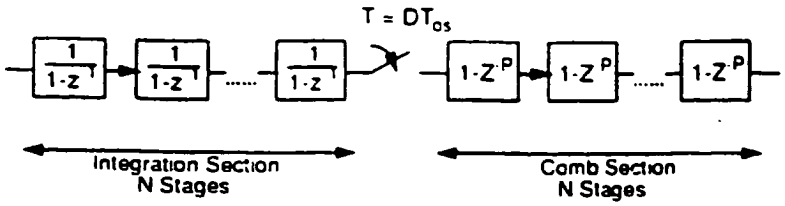


FIGURE 4.14 CIC decimation filter architecture

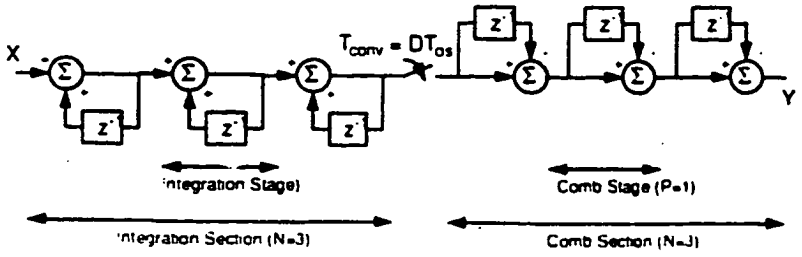


FIGURE 4.15 CIC decimation filter for N = 3, P = 1, D = 6.

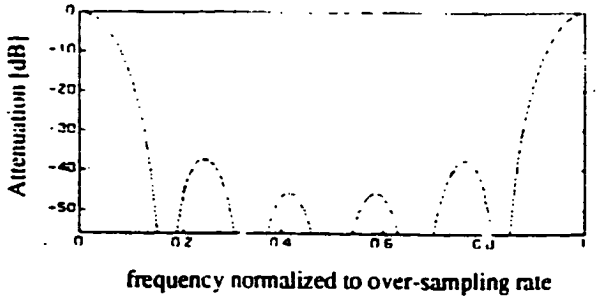


FIGURE 4.16 CIC decimation filter frequency response for N = 3, P = 1, D = 6.

$$C(z) = (1 - z^{-P})\Big|_{z = e^{j2\pi f T_{os}} = e^{j2\pi f DT_{os}}} = 1 - z^{-DP}. \qquad \text{(EQ 4.23)}$$

Cascading N integrator stages and N comb stages as illustrated in figure 4.14 results in the sinc^N transfer function H(z)

$$H(z) = I^N(z)C^N(z) = \frac{(1 - z^{-DP})^N}{(1 - z^{-1})^N} = \left[\sum_{k=0}^{DP-1} z^{-k}\right]^N. \qquad \text{(EQ 4.24)}$$

In the frequency domain this becomes

$$H(f) = \frac{(1 - z^{-DP})^N}{(1 - z^{-1})^N}\Bigg|_{z = e^{j2\pi f T_{os}}} = \left[e^{j2\pi f T_{os}(1 - DP)} \frac{\sin(\pi f T_{os} DP)}{\sin(\pi f T_{os})}\right]^N. \qquad \text{(EQ 4.25)}$$

Note that the value of DP has the effect of lengthening the impulse response of h(k) which is equivalent to narrowing the main lobe of the sinc function (i.e. inserts more zeroes in the transfer function) and therefore increases the distortion in the passband. Since D is the decimation, it can not be changed therefore P must be kept to a minimum. The remaining variable is N, the number of stages which also must be minimized as it is directly proportional to complexity and the delay of the digital filter.

Using P = 1, the value of N can be determined from the attenuation needed to suppress the out-of-band noise in the aliasing band that are BW_{DECT} wide and at multiples of f_{conv}. The attenuation required such that the noise is one bit below the SNR of 48 dB is 56 dB. Now the normalized power response CIC(f) = $|H(f)|^2/|H(0)|^2$ for P = 1 and D = 6 is

$$CIC(f) = \left[\frac{1}{D}\left(\frac{\sin(D\pi f T_{os})}{\sin(\pi f T_{os})}\right)\right]^{2N}\Bigg|_{N=3, D=6} \qquad \text{(EQ 4.26)}$$

Therefore $10\log_{10}[CIC(f_{conv} - BW_{DECT}/2)] < -56$ and solving for N gives the inequality that $N > 2.90$. Since N must be an integer, $N = 3$ is selected. The resulting frequency response for $N = 3$, $P = 1$ and $D = 6$ looks similar to figure 3.16.

Next, the output bit-length and register bit-length must be determined. The output word size B_{out} is related to the input word size B_{in} by the maximum gain possible from the transfer function H(z). Let

$$H(z) = \sum_{k=0}^{N(DP-1)} h_k z^{-k} = \left[\sum_{k=0}^{DP-1} z^{-k}\right]^N. \qquad \text{(EQ 4.27)}$$

Now the maximum possible gain can be computed from

$$G_{max} = \sum_{k=0}^{N(DP-1)} |h_k|. \qquad \text{(EQ 4.28)}$$

It is easily seen that h_k are all positive as the coefficients from the impulse response of the sinc function are all positive thus

$$G_{max} = \sum_{k=0}^{N(DP-1)} h_k = H(z)|_{z=1} = (DP)^N. \qquad \text{(EQ 4.29)}$$

Thus maximum register growth is $6^3 = 216$ and therefore with the input taking on the value of either -1 or 1 will results in an output magnitude upper bound of 216 which can represented by 9 bits (i.e. $B_{out} = 9$).

The arithmetic is that of a wrap-around system similar to 2's compliment [61]. The information stored in the register after an arithmetic operation is actually the residue of the true value and is possible as long as the output does not overflow. Let $[x]_A$ represent the residue of x modulo A with in the range [-A/2, A/2) then the output of the integrator stage v(n) using this modulo arithmetic is

$$v(n) = \left[\sum_{k=0}^{\infty} x(n-k) \right]_{A_I} \qquad \text{(EQ 4.30)}$$

applying the comb stage next

$$\begin{aligned} y(n) &= [v(n) - v(n-D)]_{A_C} \\ &= \left[\left[\sum_{k=0}^{\infty} x(n-k) \right]_{A_I} - \left[\sum_{k=0}^{\infty} x(n-D-k) \right]_{A_I} \right]_{A_C} . \end{aligned} \qquad \text{(EQ 4.31)}$$

In order for the arithmetic to be as expected, the modulo arithmetic must be the same therefore $A_C = A_I = A$ and therefore

$$\begin{aligned} y(n) &= \left[\sum_{k=0}^{\infty} x(n-k) - \sum_{k=0}^{\infty} x(n-D-k) \right]_A \\ &= \left[\sum_{k=0}^{D-1} x(n-k) \right]_A . \end{aligned} \qquad \text{(EQ 4.32)}$$

These arithmetic operations can be applied if this result matches what the original operation should have represented i.e.

$$\left[\sum_{k=0}^{D-1} x(n-k) \right]_A = \sum_{k=0}^{D-1} x(n-k) . \qquad \text{(EQ 4.33)}$$

Thus A must be chosen such that the output does not overflow. This can be extended to the whole CIC structure and therefore the arithmetic operation can be shown to be all modulo A as long as the final output does not exceed [-A/2, A/2) which gives A = 512.

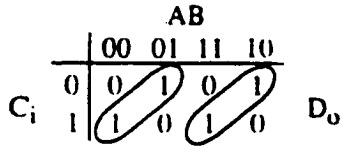
Thus the upper limit of the register word lengths (MSB)has been determined. The LSB for each register due to possible rounding/truncation is dependent upon the quantization noise. In [60], the LSB was determined at each stage by applying the principle that the variance from the error sources at each stage due to rounding/truncation of the register of

that stage should be less than the variance from the error source at the output stage due to rounding/truncation there. However, since the required output resolution is 8 bits, the noise introduced by this truncation from 9 bits to 8 bits is minimal and therefore truncation at the other stages could potentially increase the noise level above that of the 8-bit output resolution and the benefits from this would be minimal in terms of power savings as the decimator uses much less power than the baseband FIR (shown in the following pages). The results of the CIC decimator on the output of BPΣΔM with a GMSK input (see figure 4.12) is shown in figure 4.17.

The power consumption of this CIC decimator can be estimated by assuming that it is to be built from CMOS circuitry and that the power necessary to switch the state of a CMOS gate by discharging/charging its capacitive load C_{load} at a switching rate of f_{sw} and voltage supply Vss = 3V is given by

$$P = C_{load} V_{SS}^2 f_{sw}. \qquad \text{(EQ 4.34)}$$

Now a full 1-bit adder can be represented by the following Karnaugh maps for the output bit (D_o) and the carry bit (C_{out}) for inputs A and B and the input carry bit C_i



Thus

$$D_o = ((B \oplus C_i) \cdot \bar{A}) + ((\bar{B} \oplus C_i) \cdot A). \qquad \text{(EQ 4.35)}$$

Now assuming that the load capacitance of the input of an XOR gate is 0.07 pF, 0.04 pF for each AND gate, 0.04 pF for each OR gate and that in the worse case all switch states

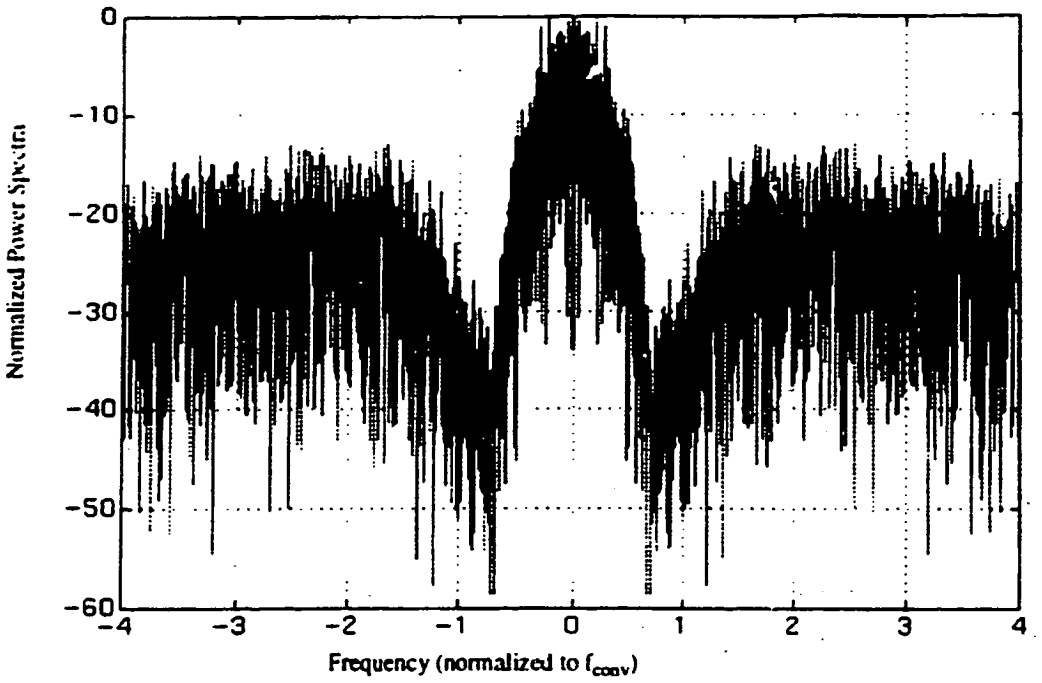


FIGURE 4.17 Output of CIC decimator on signal from BPΣΔM (with GMSK input)

then the effective capacitance that is switched is the sum of all these input capacitances = 4(0.07) + 4(0.04) + 2(0.04) = 0.52 pF. The Karnaugh map for C_{out} is

C_i \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

C_{out}

and a similar analysis gives the effective switched capacitance = 10(0.04) = 0.4 pF and therefore the total for a full 1-bit adder is 0.92 pF. A full 9-bit adder can be made by connecting 9 of these 1-bit adders together therefore the effective capacitance is 9(0.92) pF. For a data latch, this effective capacitance is 0.47 pF. Now using the fact previously derived that the maximum register size is 9-bits, the CIC decimator can be constructed from three 8-bit registers and three 9-bit adders whose states are switching at a maximum rate equivalent to the over-sampled rate f_{os} and three 9-bit registers and three 9-bit adders (assumes here that power consumption of subtract is equivalent to add) at the decimated rate f_{conv} then the power required can be estimated to be

$$\begin{aligned} P_{CIC} &= 3^2 \cdot (3 \cdot 9 \cdot (0.92 + 0.47)\,(10^{-12}) \cdot 5.296\,(10^6)) \\ &\quad + 3^2 \cdot (3 \cdot 9 \cdot (0.92 + 0.47)\,(10^{-12}) \cdot (9.216)\,(10^6)) \\ &= 21.8 \text{ mW}. \end{aligned} \qquad \text{(EQ 4.36)}$$

However further digital filtering is required to reduce the out-of-band noise from the noise shaping effects of the BPΣΔM. The power required to do this is estimated by assuming that the each stage of an N stage FIR requires an 8-bit by 8-bit multiplier, a 16-bit latch and a full 16-bit adder. Now this multiplier can be constructed from seven 8-bit adders since the binary multiplication involves shifting of bits followed by addition. Thus its effective capacitance can be estimated by 8(7)0.92 = 51.5 pF. Thus in total each FIR stage requires the charging/discharging of 74 pF capacitance. From figure 4.17, the FIR filter stop-band starts at 2.3 MHz and requires 30 dB of attenuation, the passband ends at 1.728/2 MHz and an arbitrary value of 0.1 dB passband ripple is chosen and using the Parks-Mc-

Clellan optimal equiripple design, a 13 stage FIR can be designed to produce such a response (note that this low-pass filtering takes place at the decimated rate because the decimation process has "stretched" the frequency response by the factor D and therefore the transition from the passband to the stop-band is now a greater fraction of the sampling rate f_{conv} than before decimation).

Thus the power consumption of the FIR is 80 mW for each of the in-phase and quadrature paths and therefore the total estimated power requirement for the post-processing filtering function is approximately 200 mW. This appears to be rather large but taking into account that a mobile handset will only be on once every 10 slots results in a time-averaged consumption of only about 20 mW.

4.3.11 Simulated Static BER Performance with AWGN

The complete BPΣΔADC process including the CIC decimator and baseband FIR filter was simulated using Matlab. The GMSK signal was demodulated from the baseband I and Q information in the same manner as that in [37] by obtaining the instantaneous phase from the arctangent of Q/I and then computing the phase difference from the previous symbol period for each of the 8 phases in a symbol period (from the 8 samples taken per symbol)

$$\Delta\theta_n = \theta\left(t + n\frac{T_b}{8}\right) - \theta\left(t + n\frac{T_b}{8} - T_b\right) \qquad \text{(EQ 4.37)}$$

where n = 0,1,....7 represent the 8 different phases and T_b = symbol period. The symbol timing is then recovered by finding the phase (n = 0,1,....7) where the $\Delta\theta_n$ is the largest and the symbol information is recovered by determining if the phase difference was positive (symbol = 1) or negative (symbol = -1).

The results from simulating this system in an additive white Gaussian noise (AWGN) environment is shown in figure 4.18. The performance of the system correlates well with that

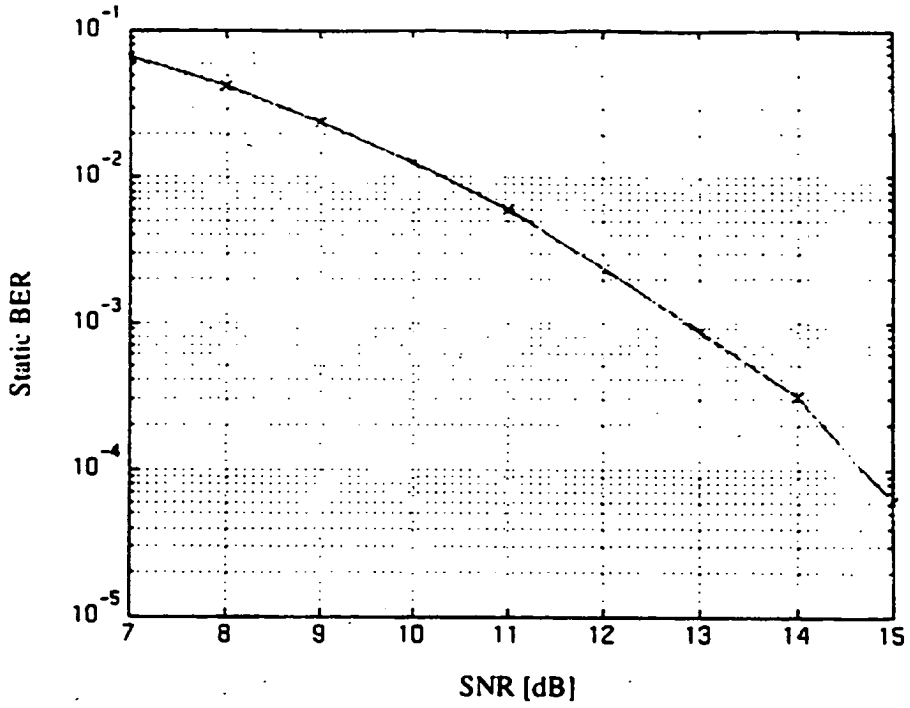


FIGURE 4.18 Simulated Static BER vs SNR performance

demonstrated by the demodulator in [37] and therefore the performance of this system in a non-fading AWGN environment has not been significantly degraded by the processing involved in using this BPΣΔM. Note that the last 2 points resulted from 5 and 1 bit errors out of 16382 bits simulated and therefore are not be statistically valid but are plotted as they do appear consistent with the downward trend of the graph. From the graph in figure 4.18 the SNR at the baseband detector that results in a BER of 10^{-3} is 13 dB. The amplitude of the GMSK signal used at the input was one-tenth that of the quantizer output. This is because the noise added during simulation at the input of the BPΣΔM has a white spectrum across the over-sampling frequency range but the actual in-band noise power is 14 dB less due to baseband filtering removing out-of-band noise. Therefore to simulate 10 dB SNR at the baseband detector, a SNR of -4 dB is required at the input to the BPΣΔM thus even if the signal alone was not saturating the BPΣΔM simulation, the noise and signal can cause saturation especially for SNR < 10 dB at the baseband detector.

4.4 COMMENTS

Although sub-sampling process allows the BPΣΔM to have a sampling rate of 55.2960 MHz, the sample-and-hold circuitry of the input stage must still be able to sample a signal centred at 124.4160 MHz accurately (note that for the stages following the input stage the signal has already been sampled and thus this requirement is not necessary). For switched-capacitor circuits, this places demands on the DC gain and unity-gain frequency of the op-amps. There are already sample-and-hold amplifiers available that can sample signals upto 700 MHz using a bipolar process [73] however they consume a lot of power (400 mW with sampling rate of 100Msps). In order to consume less power, the capacitor used to store the charge in the sampling process must be small so that less current is required to charge the capacitor. With sub-micron silicon processes available, op-amps can be designed with greater bandwidth and capacitor sizes can be reduced and an analysis of decreasing feature sizes on switched-capacitor ΣΔM [74] showed that in general

performance is improved but there is a fundamental limit to the sampling capacitor C_s reduction. Switched capacitor noise (k_BT/C_s) increases with decreasing capacitance and can affect the SNR if C_s is too small and this effect was applied to ΣΔM in [74] resulting in the following constraint on C_s

$$SNR \leq 20\log\left[\frac{V_{SUP}}{4}\sqrt{\frac{DC_s}{k_BT}}\right] \qquad \text{(EQ 4.38)}$$

where V_{SUP} = voltage supply. D is the decimation factor, k_B is Boltzmann's constant = $1.38(10^{-23})$ J/K, T is the temperature in Kelvin. Thus for D = 6, SNR = 48 dB, and a V_{SUP} = 3V, $C_s > 0.1$ fF. Thus C_s can be made small to improve speed and power requirements and yet not degrade SNR. Currently researchers are looking at Sample-and-Hold circuits (1 μm CMOS) capable of sampling signals greater than 100 MHz with 3V supplies and only consuming 10 mW of power thus a BPΣΔM with a sampling rate of 55 MHz being capable of sub-sampling a signal centered at 124 MHz and still consuming < 150 mW seems possible in the near future. Thus including the post processing functions and assuming that in a mobile handset application that the receiver is only on 1/10th of the time (since signal-strength indication is provided before the Sigma-Delta modulator) the estimated time-averaged power consumption from sub-sampling at the IF frequency to the baseband in-phase and quadrature components is 35 mW and would decrease when smaller feature sizes are available from more advanced silicon technologies (assuming that the architecture chosen allows for CMOS/BiCMOS integration).

Another factor not considered here is the aperture jitter requirement of the front-end sample-and-hold circuit of the BPΣΔM. In practice, the precise sampling instance of a sample-and-hold circuit depends not only on the internal circuitry but also on the external sampling clock used. Thus there will be some uncertainty in the exact instance in time when the signal is sampled resulting in an error (e_j) in the sampled signal level compared to the level of the signal if it was sampled at the expected instance in time.

An estimation of the aperture jitter (τ_{aj}) can be computed by assuming that the error in the signal level is random and uncorrelated [75]. The in-band SNR of the BPΣΔM with an input amplitude signal one-tenth the output amplitude of the quantizer can be seen using results from section 4.3.7 to be 38 dB. Thus from section 4.3.11, the SNR that includes the noise in the over-sampling frequency range is 38 - 14 = 24 dB. The mean-squared value of the input signal referenced to the quantizer output magnitude of 1 is 0.1^2 therefore the mean-squared value of the noise is

$$E\{e_j^2\} = \sigma_j^2 = \frac{0.01}{10^{24/10}} = 4 \cdot 10^{-5}. \qquad \text{(EQ 4.39)}$$

Using the definition of aperture jitter found in data-acquisition data books [76]

$$\tau_{aj} = \frac{\sigma_j}{(\Delta v/\Delta t)} = \frac{\sqrt{4 \cdot 10^{-5}}}{0.1\,(2\pi f_c)} = 0.01 T_c = 80 \text{ ps} \qquad \text{(EQ 4.40)}$$

where $f_c = 1/T_c$ = centre frequency of input signal = 125 MHz and $\Delta v/\Delta \tau$ is taken at the maximum rate of change of the sine wave.

4.5 CONCLUSION

The BPΣΔADC proposed here consists of a 6th order cascade-of-resonators BPΣΔM that sub-samples the GMSK signal at an IF frequency of 124.4160 MHz with an over-sampling rate f_{os} of 55.2960 MHz. The in-phase and quadrature components are then separated at this stage by a simple process of multiplication (sign inversion) of the modulator's 1-bit output (at 55.2960 Mbps) by 0,1,0,-1,0,1,.... or 1,0,-1,0,1,.... . Each of the 2 signal paths are then decimated with a 3-stage Cascaded-Integrator-Comb decimator and filtered at baseband with a 13 stage FIR resulting in the baseband I and Q digital representation that can be used to demodulate the GMSK signal.

The order of the modulator was first estimated from the sub-optimal frequency response where all the zeroes are located in the same location and an order of 6 was found to be a reasonable compromise between a high over-sampling rate and complexity. The desired

frequency response of a 6 th-order modulator was then determined through optimization of the location of the poles and zeroes of the linear approximated noise transfer function to minimize the in-band noise symmetrically about $f_{cs}/4$. A Cascade-of-resonators BPΣΔM with this linear approximated frequency response was then simulated in Matlab assuming no circuit imperfections and was demonstrated to be stable with a GMSK input. A FFT of the 1-bit output illustrated this and the expected noise shaping of the modulator. The complete BPΣΔADC including quadrature separation, CIC decimation and baseband filtering was simulated with a DECT GMSK signal of 16382 symbol periods and was demodulated from phase of the I and Q components at 8 samples per symbol (9.216 Msamples/s). The simulations demonstrated that a SNR of 13 dB or better was required to ensure that the BER was below 10^{-3} in a non-fading AWGN environment.

CHAPTER 5
RADIO-FREQUENCY FRONT-END

5.1 INTRODUCTION

The purpose of the Front-End circuitry is first to isolate the desired band-of-interest (i.e. the DECT frequency band ~ 1.9 GHz) from other interfering out-of-band signals that can be picked up over the air-waves, increase the desired signal band level while minimizing the noise added so as to make the signal more immune to any noise added to the signal processing further down the receiver chain, and then to down-convert this signal to a lower frequency (f_{IF} = 124.416 MHz) where the task of RF channel signal selection can be done with present-day technology practically.

The attenuation of out-of-band interferers is achieved with the ceramic blocking filter (see figure 3.1). This is a normally a passive device placed at the front of any receiver architecture and thus its pass-band insertion loss contributes directly to the noise figure of the system (reducing SNR). Manufacturers of these ceramic filters have designed their filters for DECT bearing this in mind and so low-loss devices (typically 1 - 2 dB worst case insertion loss) are commonly available with DECT pass-bands (1880 - 1897 MHz). Their ability to reject the interferers limits the interferers' signal strength seen by the rest of the chain reducing the dynamic range requirements on the rest of the circuits. The out-of-band interferer desensitization specifications can be found in chapter 1 and implies that a rejection of at least 20 dB at frequencies less than 1780 MHz and greater than 2000 Mhz is required such that the maximum out-of-band interferer level expected to be seen by the subsequent stage is -42.7 dBm minus the insertion loss (this rejection specification is computed from the fact that the DECT standard [10] states that the receiver must be able to operate with an interferer level of -42.7 dBm within 6 MHz of the desired RF channel and since the frequency response of these ceramic filters do not offer drastic drop-offs towards the stop-

bands then it can be correctly assumed that the subsequent stage has to at least be capable of operating with an interferer at this level of -42.7 dBm minus the insertion loss). The linearity of this device is not a concern as it is a passive element and is much more linear than the following stages and is therefore not a limiting factor in the linearity of the receiver.

The low-noise amplifier follows the blocking filter and is there to provide gain to the desired signal without introducing much noise so that the SNR is not greatly affected by the noise added in subsequent stages. This can be seen from the equation for the noise factor of two cascaded stages in Appendix B where the contribution of the noise factor of the 2nd stage is reduced if the gain of the first stage is large. Thus the goal is to achieve as much gain as possible at this stage but this is limited by the fabrication technology and also by the conflicting demands for linearity and low power consumption.

The mixer is then used to down convert the signal to the IF stage. With the LNA as a preceding stage, the noise contribution of the mixer becomes less critical. Of more importance is to maintain the linearity of the mixer so as to not produce intermodulation product levels from interferers that would degrade the reception of the desired signal. But this must again be done without reducing conversion gain too low and using too much power. The interfering effects of any energy from spurious frequencies falling in the image frequency band and mixing into the IF stage has been reduced by the attenuation at the image frequency of the blocking filter but further attenuation is required and thus a filter is placed in between the LNA and mixer to provide enough rejection and also serves to reduce any intermodulation products produced by the LNA.

This chapter describes the LNA and mixer that has been designed and fabricated in a 0.8µm BiCMOS process to work at DECT frequencies. The results from measurements made on the LNA are also presented however no measurements were made on the mixer due difficulties in using the test setup for making these measurements at these high frequencies that were identified while testing of the LNA. The test setup is described as it

ered (after a considerable amount of time and effort) to be very crucial to obtaining good results at these frequencies.

5.2 LOW-NOISE AMPLIFIER

5.2.1 General Specifications

The main requirements of the LNA were developed in chapter two and are reproduced here. The noise figure is expected to be 5.4 dB or better with a gain of 18.5 dB and an input third order intercept point of -16 dBm. There is actually some margin in this design for the noise figure, gain and intercept point as the overall receiver requirements for both the noise and linearity specification are exceeded if these targets are met thus these are the design goals. The LNA is to operate from a +3V power supply and is to consume minimal power (< 10 mA). The input and output impedance is to be 50 ohms and is necessary so that the verification of this circuit can be done directly by wafer probing (which is a 50 ohm system) without having to make a prototype board with impedance matching and transformation circuitry. From a true systems perspective, the input impedance should be such that it matches easily with the LNA and the output impedance should match to the image reject filter that follows the LNA.

5.2.2 Design Strategy

The design of amplifiers is based on the mismatching of the succeeding stages that make up the amplifier and by placing feedback around some of these stages [62]. This has resulted in many wide-band amplifiers being reported in various publications ([62,64,65,66]). However these amplifiers draw a large amount of current and do not necessarily have a low noise figure and are certainly not restricted by voltage headroom.

The constraints of low-power requirement and a single voltage supply of +3V restricts the architecture to be very simple. The 3V headroom does not allow for architectures with greater than 2 cascaded transistors without severely restricting the voltage swing of the

signal and minimizing current consumption reduces the number of stages that can be used. The reduction in current also helps to reduce the noise in the circuit (reduces the thermal and shot noise in circuit - see Appendix B) but there is a trade-off between this and the gain which would decrease reducing once again the SNR by decreasing the signal level. This simple approach was illustrated in the very few publications found on low-power LNAs operating at these frequencies ([67, 68]).

It was also decided that the RF front-end would be differential in an effort to improve immunity against power supply noise. This is necessary because the power supply rail may become rather noisy from the loading of digital circuitry. These spurious can be filtered but the amount of filtering is restricted by the amount of voltage drop that can occur across these power supply filters because it reduces the filtered supply voltage level available which is already at most 3V. Therefore the LNA would have a single input but differential outputs. However the sacrifice for this increase in the power consumption of the LNA (note that the mixer as a gilbert cell is inherently differential and that differential SAWs are available).

Thus to summarize, the strategy is to produce a simple single-input differential output design with the primary concern being the noise figure, gain and power consumption. The input and output impedance is to be matched as close to 50 ohms as possible but is considered secondary. The linearity is also considered secondary and the trade-off between linearity and noise figure (without sacrificing power consumption) is to be explored by fabricating variants to the LNA design that has improved linearity circuitry such as emitter degeneration.

5.2.3 The LNA circuit and description

The circuit diagram for the LNA is shown in figure 5.1. The single input stage consists of a common emitter amplifier with shunt feedback (transimpedance amplifier). A common base configuration was rejected even though the noise seen at the input is less (the emitter

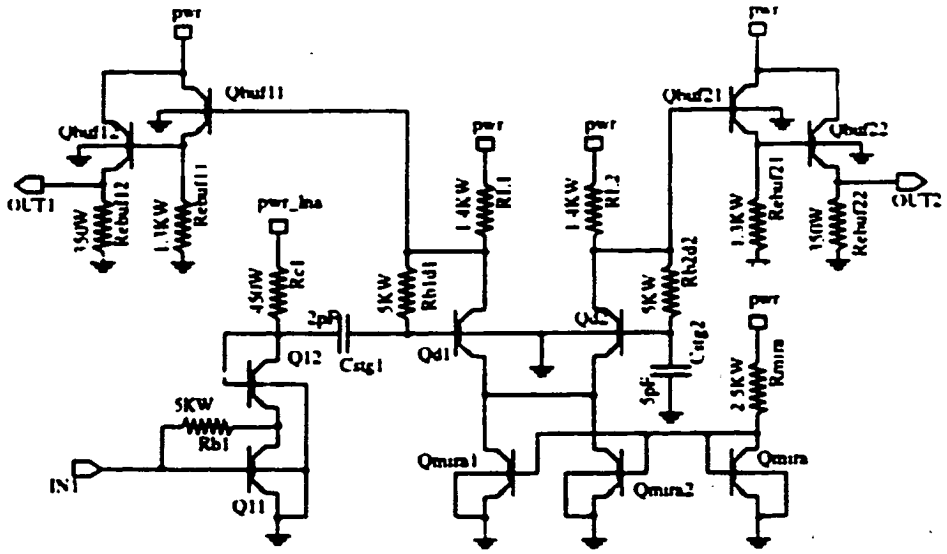


FIGURE 5.1 LNA circuit diagram

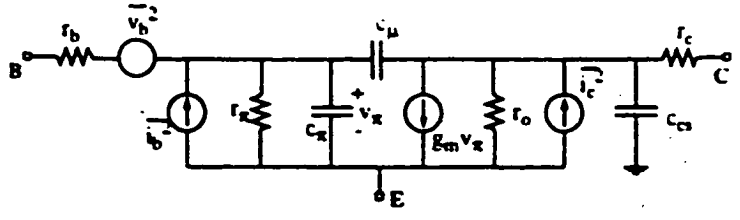


FIGURE 5.2 Equivalent Circuit for BJT including noise sources

intrinsic resistance is less than the intrinsic base resistance which improves the thermal noise seen at the input due to this input resistance - see Appendix B) because the improvement in the noise performance is overshadowed by the degradation in the first stage gain due to the mismatch from the low input impedance of the common base configuration. The second stage is a differential pair with one side grounded to provide the conversion from single ended to differential and is followed by a emitter follower to convert the la · output impedance of the 2nd stage to a lower 50 ohms.

The main contributions to the noise level in the transistor occurs in the first stage as expected (see Appendix B). This can be seen by assuming that the r..stors including the intrinsic resistance within the transistor are thermal noise sources and the bipolar transistor's collector-base and emitter-base junctions give rise to shot noise sources [69] (see figure 5.2). Their overall effect on the noise depends on the transfer function from the noise source to the output and this implies that the intrinsic resistance r_b of transistor Q11 directly adds to the output as noise source is right at the input to the LNA. Therefore r_b of Q11 must be kept to a minimum value and this is done through the selection of different sized transistors. Transistors with larger emitter areas have smaller base resistance as they have a larger surface area that is in contact with the base reducing r_b. However, a larger transistor results in larger parasitic junction capacitances and this reduces the bandwidth of the amplifier. The optimal transistor size was found so that the noise figure could be below 5 dB and still yield a good gain. A reasonable first stage gain is required to minimize the contributions from the remaining stages even though it increases the Miller capacitance [70].

Transistor Q12 is used to drop some voltage across it without having to use a large resistance and is used to reduce the reverse bias across the base-collector junction reducing the parasitic capacitance. This also helps to reduce the feedback resistance that is used to set the bias of the first stage transistors but cannot be reduced too low as it would reduce the

input impedance too much as well. In accordance with Miller's theorem [70], the effective resistance of the feedback resistance R_{b1} seen at the base is reduced and this also improves the noise performance.

The first and second stage are interconnected via a coupling capacitor so that the DC operating point of the second stage differential pair is not affected by the first stage. Ideally the best way of ensuring balance of the operating point is to duplicate the first stage on the Qd2 side but this would results in an increased power consumption.The second stage differential pair (Qd1, Qd2) is biased using the current mirror created by Qmira, Qmira1and Qmira2 (the bias current is set by the voltage at node Vb).The gain of this stage is not large so that the Miller capacitance does not overwhelm the performance. The size of the transistors, although not as critical to the overall noise of the circuit as that from Q11 and Q12, was found to degrade the noise figure if they were too small. In order to improve linearity, a variant of this circuit with emitter degeneration R_e in the differential pair was also fabricated.

The last stage is an emitter follower used to convert the high impedance seen at the output of the differential pair to a much lower 50 ohms. The concern here was to minimize the power consumption without limiting the voltage swing at the output (set by the DC voltage level at the emitter of Qbuf12 and Qbuf22), increasing the output impedance too high or reducing the bandwidth of the follower.

HSPICE circuit simulations of the LNA were performed including equivalent circuit models of bond wires (inductances of 1 nH) and the bonding pads which were modelled as a capacitor (0.2 pF) and resistor (200 Ω) in series to ground. The source and load impedances were assumed to be 50 Ω. Another simulator, ELDO was used to finalize some component values by optimizing the performance of the circuit with respect to minimizing noise and maximizing gain while being constrained to 50 Ω input and output impedances.

Simulated results @ 1.9 GHz

Noise Figure = 4.5 dB

Gain = 18.7 dB

Power @ 3V = 24 mW

IIP3 = -20 dBm

Zin = 39 - 16j Ω

Zout = 47 + 40j Ω

The LNA was fabricated using Northern Telecom's 0.8 µm BiCMOS process.

5.2.4 Layout Considerations

Primarily the layout of the circuit depended upon how the circuit is to be tested. If the circuit is to be packaged, the layout would be such that the input and output distance from the pads to the actual package pins are minimized as this reduces the inductance of the bond wires by minimizing their lengths. If the circuit is to be wafer probed the layout of the pads are fixed to match the geometry of probe contact. Since the LNA is a relatively small circuit with few bonding pads the layout was designed such that it could be packaged or wafer probed.

The 8 contact probe that is to be used in testing has its 8 contacts arranged as

PSSGGSSP (see figure 5.5)

where P is a power contact (i.e. has decoupling capacitor to ground very close to the contact point and is therefore only useful for DC signals), S is a signal line and G is for ground and the contact is grounded directly. This arrangement provides a shielding ground for each signal line from the probe down to the wafer reducing coupling and other parasitic effects. Therefore to be able to wafer probe the circuit, the pads would have to be arranged this way.

Other useful layout practices:

- Minimize resistance from power supply and ground pads to circuit by using wide metal contact strips.
- maximize distance between input and output areas so as to reduce coupling.
- keep transistors especially those that are to be matched (e.g. in differential pairs) as close as possible so as to minimize process variation between them.
- surround circuits with a ground ring of a metal layer that is connected to substrate through minimally spaced contact vias. This helps to shield the circuit.
- place Q11 as close to the input bonding pad as possible.

5.2.5 Verification

The LNA parameters tested are:

Noise Figure

Gain

Input and Output impedance

Third-Order Intercept Point

The testing of the LNA is done by wafer probing the circuit using a Cascade Microtech Summit Probe station which allows the user to make electrical contact with the bonding pads directly by lowering a Cascade Microtech 8 contact probe such that its 8 gold contacts are physically touching the 8 pads. The electrical signal from the probe contact is then transmitted through a 50 ohm microstrip line to an SMA connector where various signal generators and instrumentation can be attached.

First, the input and output impedance of the LNA were measured using a network analyzer as it also ensures that the contact probe is making good contact with the bonding pads before measuring the noise figure. The output of the LNA is differential and since most instruments have only one input and/or output port, the differential output has to be combined and this is achieved through the use of a 3 dB coupler. The monitoring of the output impedance therefore is more difficult but it was found to be sufficient to monitor the impedance of just one of the output ports and then very carefully physically reconnect it to the 3 dB coupler while constantly monitoring the input impedance.

With the confirmation of good physical contact between the probe and the bonding pads, the noise figure of the LNA is measured by switching over the connections between the network analyzer and the noise figure meter (see figure 5.4). RF switches are used to ensure that the connections were not physically disturbed because it was found that vibrations caused by physically reconnecting the cables (attached at one end to the probe) from the network analyzer to some other instrumentation may results in a bad contact affecting results. This procedure was also followed when conducting the two-tone intermodulation measurements. The connections to the 8 contact probes are shown in figure 5.5.

S_{21} is the forward transmission coefficient and is defined as the ratio of the power incident upon the load to the power incident upon the input of the LNA when the source and load are non-reflecting (i.e. matched). Measuring the S-parameters of the LNA accurately by using the network analyzer directly is not possible as the circuit is essentially a three-port device. However the S-parameters for the two-port network where one of the output port is terminated to 50 ohms were measured and since the output impedance of these ports are relatively close to 50 ohms, therefore any reflections back into these ports are considered negligible. The input and output impedance from these measurements (S_{ii}) therefore are reasonable estimates of what they would be if ports were match-terminated. The S_{21} results from the two-port network where one of the output ports is terminated are power

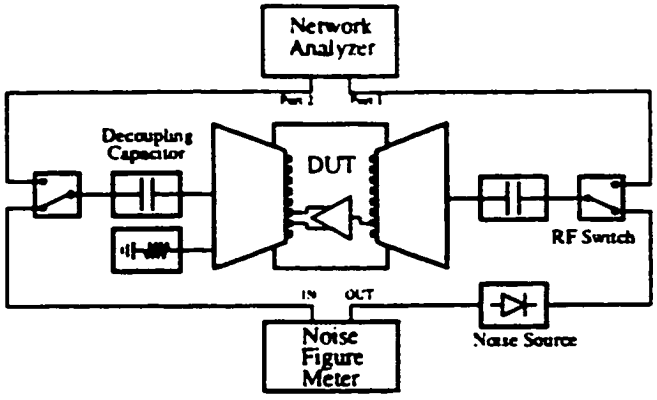


FIGURE 5.3 Single-input Single-output LNA Test set-up

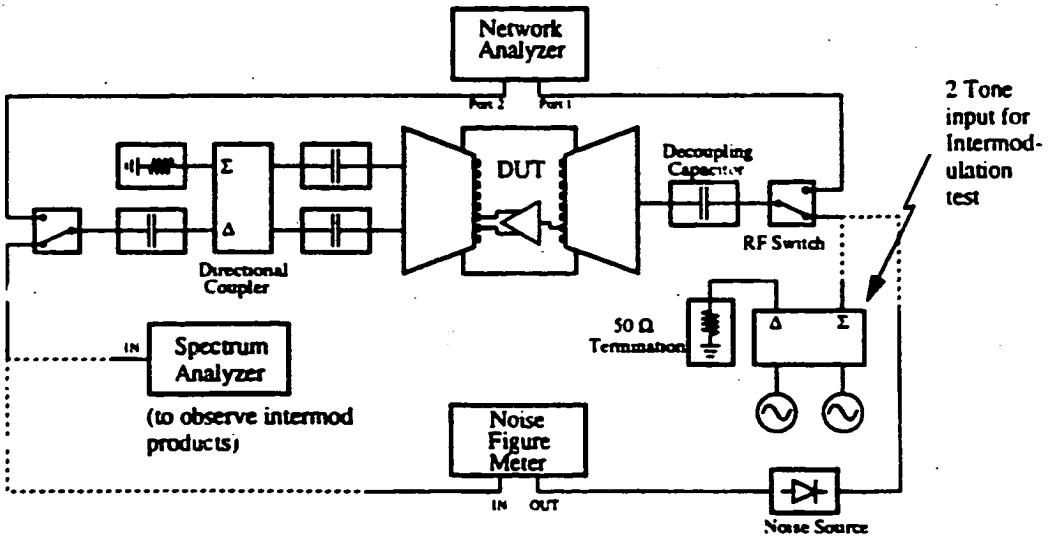


FIGURE 5.4 Single-input Differential-ouput LNA Test set-up

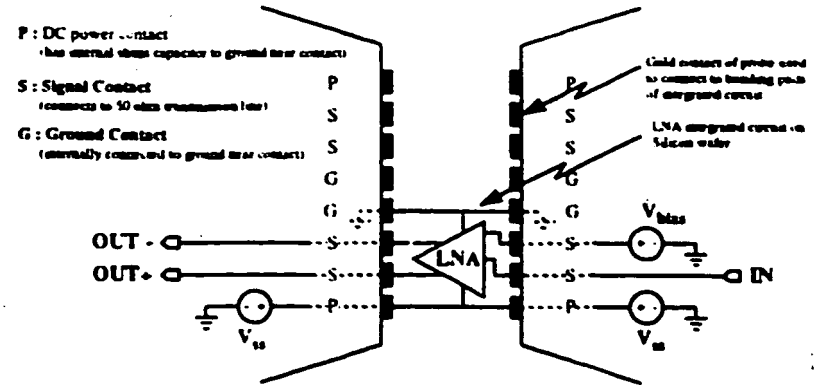


FIGURE 5.5 Close-up view of Cascade Microtech Probe illustrating connections to integrated circuits

combined differentially to give the estimate of the overall forward transmission coefficient i.e. $|S_{21}|^2_{LNA} = |S_{21}|^2_{out1} + |S_{21}|^2_{out2}$.

The noise figure was measured using the Rhodes & Schwartz spectrum analyzer noise figure setup on the duo output port test setup so that the combined noise from both output ports can be measured. The noise figure of the LNA alone has to be computed from the NF measured by the spectrum analyzer by taking into account the cabling and connections between the noise source and LNA (cable loss was 2.2 dB at 1.9 GHz contributes directly to the NF measured) and also the cabling from the LNA to the analyzer's input (contributes less to overall noise measured as the gain of the LNA is high enough).

5.2.6 Results

5.2.6.1 Circuit A (LNA without emitter degeneration)

Linearity: The third-order intercept point is measured by applying two tones into the input of the LNA and then observing the level of the 3rd order intermodulation products produced on either side of the two original tones spaced equally apart.

Output power of each 2 tones = -27.07 dBm

Output power of each IM product = -75.07 dBm

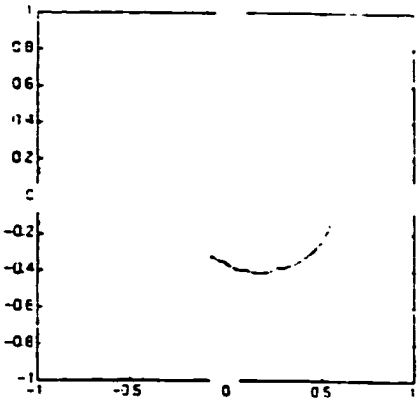
Therefore

OIP3 of LNA @ 1.9 GHz = -3.07 dBm.

Power:

Vpwr = 3 V,	Ipwr = 4.5 mA.
Vb = 3 V,	Ib = 0.85 mA.
Vpwr_lna = 3 V,	Ipwr_lna = 2.5 mA.

Total power = 23.5 mW.



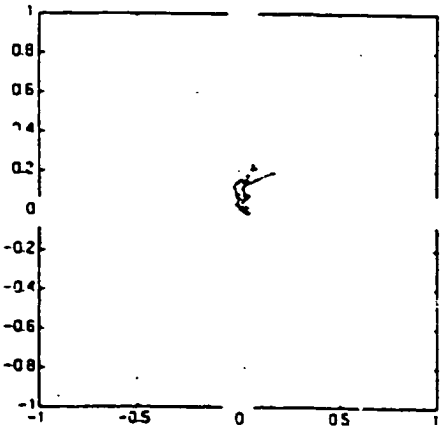
Input Impedance:

Z_{in} @ 1.9 GHz = 37 - 25 j Ω

Input Return Loss @ 1.9 GHz = 9.33 dB

Input VSWR @ 1.9 GHz = 2.0

FIGURE 5.6 Smith Chart of Input Impedance for Circuit A



For Output Port 1:

Z_{out1} @ 1.9 GHz = 64 + 23 j Ω

Output Return Loss @ 1.9 GHz = 12 dB

Output $VSWR_{out1}$ @ 1.9 GHz = 1.67

For Output Port 2:

Z_{out2} @ 1.9 GHz = 55 + 23 j Ω

Output Return Loss @ 1.9 GHz = 13 dB

Output $VSWR_{out2}$ @ 1.9 GHz = 1.57

FIGURE 5.7 Smith Chart of Output Impedance for Circuit A

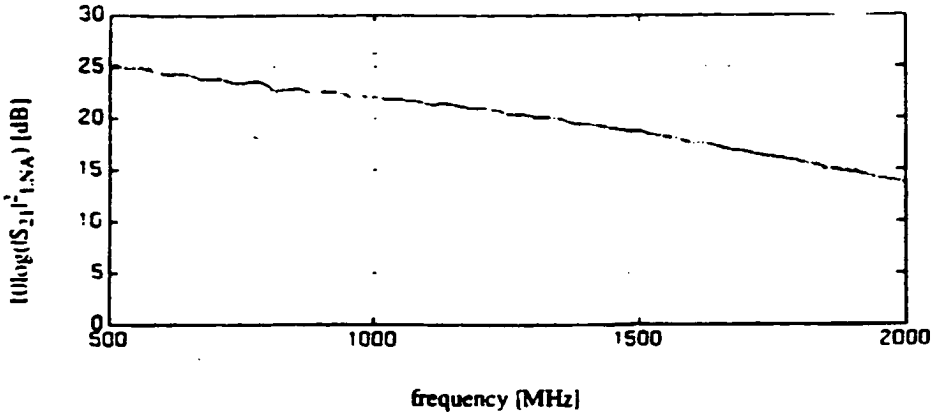


FIGURE 5.8 Gain vs Frequency for Circuit A

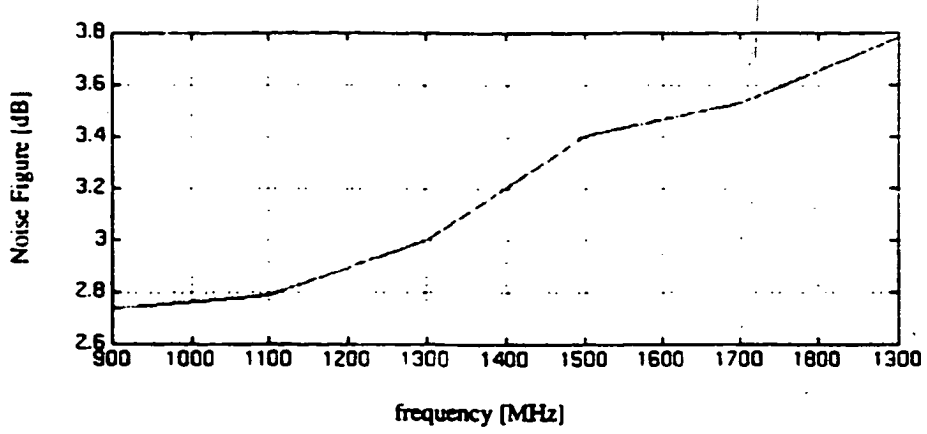


FIGURE 5.9 Noise Figure vs Frequency for Circuit A

5.2.6.2 Circuit B (LNA with R_e for emitter degeneration = 100 Ω)

Linearity: From output spectrum using Rhodes & Schwartz spectrum analyzer at combined output while applying two tones into the input of the LNA

Output power of each 2 tones = -26.07 dBm

Output power of each IM product = -77.07 dBm.

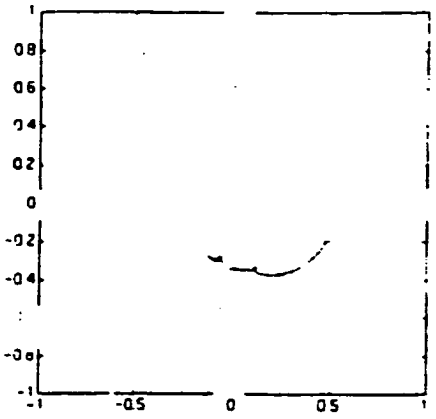
Therefore

OIP3 of LNA @ 1.9 GHz = -0.57 dBm.

Power:

Vpwr = 3 V.	Ipwr = 4.4 mA.
Vb = 1.83 V.	Ib = 0.53 mA.
Vpwr_lna = 3.15 V.	Ipwr_lna = 2.1 mA.

Total power = 22.0 mW.



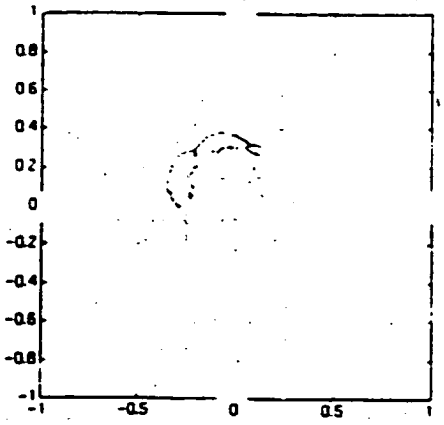
Input Impedance:

Z_{in} @ 1.9 GHz = 35 - 20 j Ω

Input Return Loss @ 1.9 GHz = 10.9 dB

Input VSWR @ 1.9 GHz = 1.8

FIGURE 5.10 Smith Chart of Input Impedance for Circuit B



For Output Port 1:

Z_{out1} @ 1.9 GHz = 52.5 + 36 j Ω

Output Return Loss @ 1.9 GHz = 9.6 dB

Output $VSWR_{out1}$ @ 1.9 GHz = 2.1

For Output Port 2:

Z_{out2} @ 1.9 GHz = 50 +32.5 j Ω

Output Return Loss @ 1.9 GHz = 10.6 dB

Output $VSWR_{out2}$ @ 1.9 GHz = 1.85

FIGURE 5.11 Smith Chart of Output Impedance for Circuit B

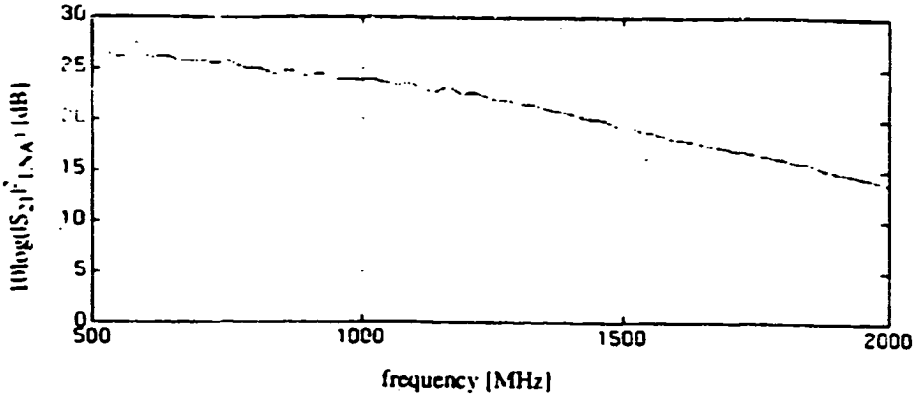


FIGURE 5.12 Gain vs Frequency for Circuit B

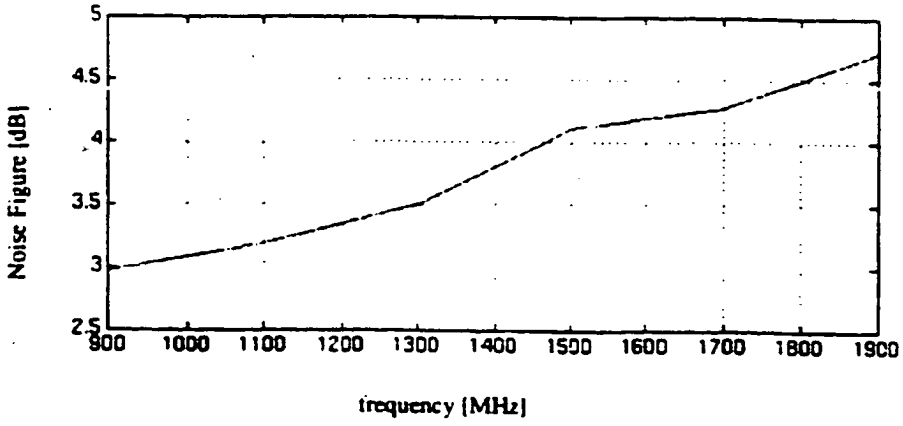


FIGURE 5.13 Noise Figure vs Frequency for Circuit B

5.3 MIXER

Two designs were fabricated: the first design is a standard gilbert cell multiplier and the second design involves linearizing the differential pair in the gilbert cell to improve the linearity.

5.3.1 General Specifications

The main requirement for the mixer is to have conversion gain to minimize the effects on noise from following stages and to be linear to reduce the interference from intermodulation products. The noise figure requirement is much more relaxed because of the LNA in front of the mixer with its high gain. The power requirements are just as critical and must be minimized and it is to operate at 3V. The input impedance is expected to be 50 ohms as it must interface with the SAW and LNA and the output impedance is designed to be 200 ohms.

5.3.2 Standard Gilbert Cell Multiplier

The exact analysis of a Gilbert cell can be found in many text [69, 70] and is reproduced here briefly. The operation of the Gilbert cell stems from the relationship between the current and voltage across a differential pair which can be written as

$$\Delta I_c = I_{c1} - I_{c2} = I_{EE}\tanh(V_d/2V_T)$$

where V_T is the threshold voltage of the 2 matched transistors. Now this expression can be simplified assuming $V_d/2V_T << 1$ to

$$\Delta I_c = I_{EE}(V_d/2V_T).$$

Thus by varying I_{EE} proportionally with one input multiplicand and varying V_d proportionally with the other multiplicand, ΔI_c would represent the results of multiplying the two inputs together. In figure 5.15 the transistor Qmix1 and its emitter resistance R_{e1} converts the input voltage applied at its base to a collector current proportional to this voltage that

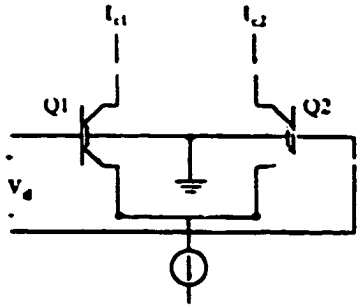


FIGURE 5.14 Differential pair

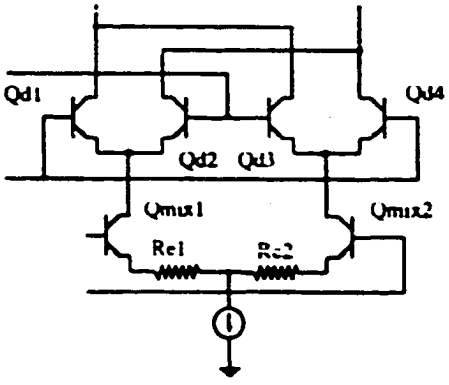


FIGURE 5.15 Gilbert cell multiplier

can be used to drive the differential pair R_{e1} provides emitter degeneration to linearize this process but can not be too large as the transconductance ($\sim 1/R_{e1}$) becomes too small reducing the gain and also shift the voltage level of the nodes in the differential pair higher restricting output swing.

The differential pair in figure 5.14 can not be linearized using emitter degeneration because emitter degeneration causes the transconductance to be proportional to conductance of the emitter resistance and therefore independent of V_d thus no multiplication effect occurs.

The circuit is shown in figure 5.15 and is a standard gilbert cell. Simulation gave the following results for an RFLO voltage amplitude of 200 mV differential:

IIP3 = + 2.4 dBm

Voltage Gain = 3.5

Current = 4 mA

The layout guidelines of section 5.2.4 was followed.

5.3.3 Gilbert Cell Linearization by transistor mismatch

The differential pair can be linearized by combining mismatched differential pairs [71, 72]. The transconductance $G(V_{in})$ of the combination of all the differential pairs shown in figure 5.16 can be written as [72]

$$G(V_{in}) = \sum_{k=1}^{floor(N/2)} \alpha_k \{ g_m(V_{in} - V_k) + g_m(V_{in} + V_k) \} + \beta g_m(V_{in}) \quad \text{(EQ 5.1)}$$

where $g_m(V_{in}) = d(\Delta I_c)/dV_{in}$ is the transconductance for a differential pair and N is the number of differential pairs operating in parallel ($\beta = 0$ for N even). V_k is the DC offset applied to one side of the pair (the overall transconductance is still dependent on the voltage across the bases of the linearized pair, V_{in} and thus can be used in the Gilbert cell.

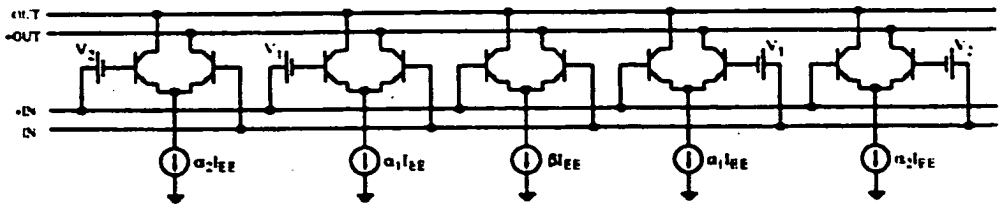


FIGURE 5.16 Combining differential pairs with voltage offsets (K = 2)

N	$V_1/2V_T$	$V_2/2V_T$	α_1	α_2	β	G(0)/G(0, N=1)
1	-	-	-	-	1.0	1.0
2	0.6585	-	1.0	-	-	0.667
3	1.0317	-	1.0	-	0.64	0.545
4	0.3541	1.2978	0.5479	1.0		0.480

TABLE 5.1 Differential pair linearization parameters

Therefore to linearize this circuit, the function $G(V_{in})$ must be constant or maximally flat and this is done by setting the derivatives of $G(V_{in}) = 0$

$$G^{(2)}(0) = G^{(4)}(0) = \ldots\ldots = G^{(2(N-1))}(0) = 0 \qquad \text{(EQ 5.2)}$$

note that $G(V_{in})$ is even therefore all odd derivative equal 0 when evaluated at 0). The results of this analysis was performed in [72] and resulted in the values in table 5.1. Notice from the last column that the transconductance although it becomes more linear does reduce in value (i.e. less conversion gain).

The DC offset V_k is produced by mismatching the sizes (emitter-base junction area) in the differential pair. The saturation current of a BJT is proportional to this area thus if Q1 of the kth differential pair (figure 5.16) has an emitter-base junction area m times greater than Q2 then its saturation current will also be m times that of Q2. Thus if offset V_k is to be applied to transistor Q1

$$\begin{aligned} I_{c1} &= I_s \exp[(V_{be1} + V_k)/V_T] \\ &= mI_s \exp(V_{be1}/V_T) \end{aligned}$$

where $m = \exp(V_k/V_T)$. Figure 5.17 shows the equivalent linearized differential pairs for N = 2 where $m = \exp(2(0.6585)) = 3.73$.

This is used to replace the upper differential pairs in the Gilbert cell. Higher values of N are not used even though they provide a greater range of linearization for input V_{in} because the number of transistors required increases and the values of α_k increase and this results in larger transistor that would require more current. The actual value for m used is 4 because only discrete values of m is available in this process.

The complete linearized Gilbert Cell is shown in figure 5.18. Simulation gave the following results for an RFLO voltage amplitude of 200 mV differential:

$$IIP3 = +4.4 \text{ dBm}.$$

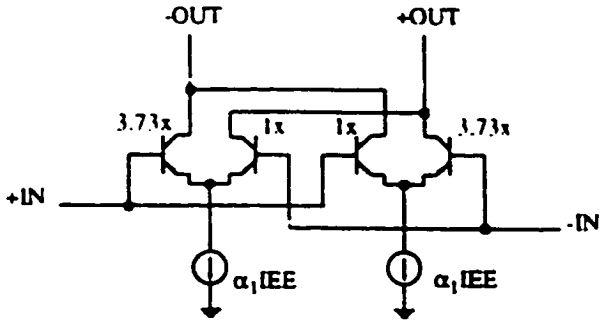


FIGURE 5.17 Linearized differential pair with N = 2

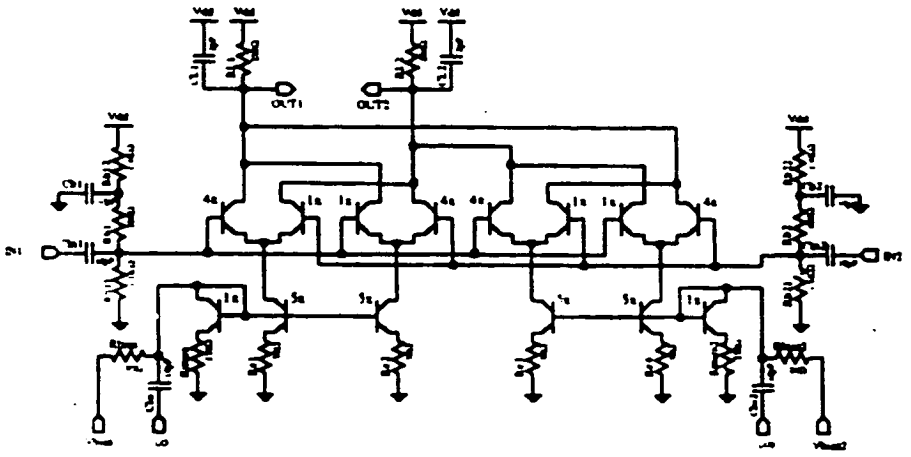


FIGURE 5.18 Circuit diagram for Linearized differential pair with N = 2

Voltage Gain = 1.11.

Current Consumption = 10 mA (Vdd = 3V, Vbias = 1.82 V).

The layout guidelines of section 5.2.4 was followed particularly the need for matching.

5.3.4 Comments

There is not much improvement in IIP3 from simulations but the circuits were still fabricated just to verify this. However due to the state of the 8 contact probe (from experience of probing LNA), it does not seem possible to be able to get good contact on all bonding pads therefore in order to test the mixer, the circuit would have to be packaged.

The linearized mixer does not appear to offer a great enough improvement in IIP3 over the standard Gilbert cell mixer to warrant the extra power consumption. It would probably be more useful in a system where there was not such a harsh restriction on the power consumption and power supply rails allowing an N > 2 to be used.

5.4 CONCLUSION

Designs for a low-power, low-voltage LNA and a low-power, low-voltage mixer have been presented here. Thee designs were simulated and fabricated in Northern Telecom's 0.8 µm BiCMOS process. However only the LNA was verified through measurements to exceed the simulated results. The mixer could not be wafer probed due to the condition of the 8-contact probe available.

The NF results of the LNA were found to [illegible] and because the NF of the LNA was lower than expected, the LNA [illegible] eration (Re = 100 ohms) which gives a higher OIP3 (and therefore high[illegible] can be used in the receiver and still meet the noise performance requirements. Thus these parameters will be used in chapter six. The wafer probed measurements are slightly different from the simulated results as the measurements do not have the bond wires present and therefore the inductance of the

bond wires are not included. The measured input impedance of the LNA was capacitive however if the bond wire inductance of the at the input was included in series the resulting impedance would actually be less capacitive and almost purely resistive. For the output impedance, the bond w : : connection from the output pads to the output pins would result in a more inductive impedance. The NF was found to be better because the semiconductor process parameters had slightly improved compared to the models used in the simulation.

CHAPTER 6
CONCLUSION

A single-IF DECT receiver architecture has been presented here that converts a DECT GMSK signal at 1.9 GHz to its baseband I and Q components at 8 times the symbol data rate (for asynchronous demodulation [37]) and was estimated to consume only 41 mW (assuming from the previous chapters that the receiver is only powered every 10 TDMA slots and that the RF front-end requires 36 mA, the IF limiter 8 mA at 3V and the BPΣ–ΔADC time-averaged consumption is 35 mW). The baseband I and Q components were successfully demodulated using a technique similar to that in [37] resulting in good performance even in a additive white Gaussian noise environment.

The DECT standard was found to be not very demanding, because of its intended application and its use of TDMA/FDMA, on the RF sensitivity, intermodulation and spurious interference desensitization when compared to cellular standards and this allows some flexibility in the choice of receiver architecture. For these reasons, a multiple-IF architecture did not seem necessary as it also increases the number of components and cost. A zero-IF architecture although attractive appeared also to be too difficult and not suitable particularly because of the wide bandwidth of a DECT RF channel making the baseband circuitry susceptible to commercial radio broadcasts in the AM band. Thus an single-IF system was chosen as a compromise.

The single-IF architecture proposed in chapter 3 used a quadrature sub-sampling process to produce a receiver that could convert the IF analog signal to the digital domain at the IF stage making the receiver more robust and manufacturable due to the reduction of analog signal processing circuitry. The sub-sampling allows for the sampling of a bandlimited signal at a sampling rate lower than the bandlimited signal's centre frequency and with proper selection of sampling rates and IF frequency, the quadrature separation in the digi-

tal domain becomes a trivial process and results in no I and Q gain or phase imbalance. The lower limit of the sampling rate of the converter was found to be restricted by the rejection of the replicas produced during quadrature separation at half the sampling rate and also by the image frequency bands also a half the sampling rate.

The IF frequency was lower bounded by the RF Image rejection abilities of the RF Image reject filter and by the IF SAW, and upper bounded by the achievable gain of the IF stage which needed to have a high gain so as to reduce the noise contributions from the ADC while being constrained on power consumption.

A BPΣΔADC was used as the ADC because they inherently sample narrow-band signals at a non-zero centre frequency, have a high sampling rate and has a band-pass frequency response. They can be fabricated in silicon technologies and low-pass ΣΔM with 50 MHz sampling rate have been constructed that consume less than 50 mW. Their 1-bit output also extremely simplifies the process of quadrature separation.

In chapter 4, it was found that a 6th-order cascade-of-resonators BPΣΔM with a over-sampling rate of 55.2960 MHz was able to sub-sample the DECT GMSK signal of 1.728 MHz bandwidth centred at 124.4160 MHz with the necessary in-band SNR of 48 dB. Because the SNR required is much lower than that normally designed for in ΣΔM (particularly the low-pass versions), the resulting complexity and over-sampling rate is reduced making this practically more implementable at these frequencies. The frequency response of the modulator was determined through optimization of the locations of the poles and zeroes of the linearized noise transfer function. Decimation process involved a cascaded-integrator-comb (CIC) decimator followed by a 13 stage FIR baseband filter.

The complete BPΣΔADC including quadrature separation, CIC decimation and baseband filtering was simulated with a DECT GMSK signal of 16382 symbol periods and was demodulated from phase of the I and Q components at 8 samples per symbol (9.216 Msam-

ples/s). The simulations demonstrated that a SNR of 13 dB or better was required to ensure that the BER was below 10^{-3} in a non-fading AWGN environment. The time-averaged power consumption of the BPΣΔADC was estimated to be 35 mW (assuming that the its is powered every 10 TDMA slots).

A Low-Noise amplifier (LNA) and mixer was designed and fabricated in chapter 5 and the performance of the LNA was determined from wafer probing the integrated circuit and was found to provide a gain of 14 dB and an output 3rd-order intercept point of -0.5 dBm with only a noise figure of 4.7 dB and consuming only 22 mW with a 3V power supply. Another variant provided better noise performance but had less linearity for the same amount of power consumed demonstrating the trade-off available.

The final noise, gain and linearity budget for the receiver is shown in table 6.1 and incorporates the actual measured values for the LNA and the simulated values for the mixer. There is about 3 dB of margin on the overall NF performance and the linearity (intercept point) has about 6 dB of margin due to the lower gains of the LNA and mixer.

All the specifications in table 6.1 of the various components required in this receiver were derived from actual currently available parts and devices except for the BPΣΔM as this component is not available yet. There is currently on going research into developing BPΣΔM with higher over-sampling rates and better resolution but the sampling rate of the BPΣΔM required for this receiver is modest (55.2960 MHz) and there are already LPΣΔM that have higher sampling rates (and consumes low power). The resolution requirement is also very modest at 6 bits (with no margin for degradation). A definite area for further research is in the implementation of the specified BPΣΔM. The architecture and its coefficients have already been defined in chapter 4 however the circuitry of the individual blocks particularly the 100 MHz sub- sample-and-hold circuit (to be distinguished from a 100 Msps sample-and-hold circuit) have not been determined. Other circuit non-idealities like the effects of clock jitter on the sampling at the IF frequency and the effects on the

BER performance with component tolerances in a silicon fabrication process would require further investigation.

	INDIVIDUAL			CUMULATIVE			
Component	Gain [dB]	NF [dB]	OIP3 [dBm]	Gain [dB]	NF [dB]	OIP3 [dBm]	IIP3 [dBm]
Ceramic Filter	-2	1	100	-2	1.0	100	102
Duplexor	-1	1	40	-3	2.2	40	43
LNA	14	4.7	-0.5	11	7.45	-0.5	-11.5
Ceramic Filter	-2	1	100	9	7.47	-2.5	-11.5
Mixer	4.8	17	2.4	13.8	10.7	-0.7	-14.5
SAW	-12.5	4	100	1.3	10.7	-13.2	-14.5
Limiting Amplifier	70	8	-	71.3	12.0	-	-
LPF	-2	2	100	69.3	12.0	-	-
ADC	-	77	-	-	13.4	-	-

TABLE 6.1 Final Link Budget for DECT Receiver

APPENDIX A: DECT Glossary

Bearer (MAC bearer)	MAC bearers are the service elements that are provided by each Cell Site Function (CSF). Each bearer corresponds to a single service instance to the physical layer. See also simplex bearer, duplex bearer and double simplex bearer.
Bearer handover	the internal process provided by the MAC layer, whereby one MAC connection can modify its underlying bearers while maintaining the service provided to the DLC layer. NOTE: bearer handover is slot based.
Broadcast	a simplex point-to-multipoint transmission. NOTE: the transmitter may disregard the presence or absence of receivers.
Cell	the domain served by a single antenna(e) system (including a leaky feeder) of one FP. NOTE: a cell may include more than one source of radiated RF energy (i.e. more than one REP).
Connection handover	the internal handover process provided by the DLC layer, whereby one set of DLC entities (C-plane and U-plane) can reroute data from one MAC connection to a second new MAC connection, while maintaining the service provided to the network layer. NOTE: Connection is DLC frame based.
Double simplex bearer	the use of two simplex bearers operating in the same direction on two physical channels. These pairs of channels shall always use the same RF carrier and shall always use evenly spaced slots (i.e separated by 0.5 TDMA frame).
Down-link	Transmission in the direction of FT to PT
Duplex bearer	the use of two simplex bearers operating in opposite directions on two physical channels. These pairs of channels shall always use the same RF carrier and shall always use evenly spaced slots (i.e separated by 0.5 TDMA frame).
External handover	the process of swiching a call in progress from one FT to another FT

Fixed Part	FP	a physical grouping that contains all of the elements in the DECT network between the local network and the DECT air interface NOTE: an FP contains logical elements of at least one FT plus additional implementation specific elements.
Fixed radio Termination	FT	a logical group of functions that contains all of the DECT processes and procedures on the fixed side to the DECT air interface. NOTE: a fixed radio termination only includes elements that are defined in ETS 300 175. This includes radio transmission elements (layer 1) together with a selection of layer 2 and layer 3 elements.
Full Slot (Slot)		one 24th of a TDMA frame which is used to support one physical channel.
Handover		the process of switching a call in progress from one physical channel to another physical channel. These processes can be internal (see internal handover) or external (see external handover). NOTE: There are two physical forms of handover, intra-cell handover and inter-cell handover. Intra-cell handover is always internal, inter-cell handover can be internal or external.
Inter-cell handover		the switching of a call in progress from one cell to another cell.
Internal handover		handover processes that are completely internal to one fixed radio termination. Internal handover reconnects the call to the lower layers, while maintaining the call at the Network layer. NOTE: the lower layer reconnection can either be at the Data Link Control layer (see connection handover) or at the Medium Access Control layer (see bearer handover).
Logical Channel		a generic term for any distinct data path. Logical channels can be considered to operate between logical end points.
MAC connection (connection)		an association between one source MAC Multi-Bearer Control (MBC) entity and one destination MAC MBC entity. This provides a set of related MAC services (a set of logical channels), and it can involve one or more underlying MAC bearers.
Multiframe		a repeating sequence of 16 successive TDMA frames, that allow low rate or sporadic information to be multiplexed (e.g. basic system information or paging)
Normal Transmitted Power	NTP	transmitted power averaged from the start of bit 0 of a physical packet (e.g. P32) to the end of the physical packet.

Paging		the process of broadcasting a message from a FP to one or more PPs. NOTE: different types of paging messages are possible e.g. the {Request Paging} message orders the recipient to respond with a call set-up attempt.
Physical Channel (channel)		the simplex channel that is created by transmitting in one particular slot on one particular RF channel in successive TDMA frames. See also simplex bearer.
Portable Part	PP	a physical grouping that contains all elements the user and the DECT air interface. PP is a generic term that may describe one or several physical pieces. NOTE: a PP is logically divided into PT plus one or more portable application
Portable radio Termination	PT	a logical group of functions that contains all of the DECT processes and procedures on the portable side of the DECT air interface NOTE: a PT only includes elements that are defined in ETS 300 175. This includes radio transmission elements (layer1) together with a selection of layer 2 and layer 3 elements.
Radio End Point	REP	a physical grouping that contains one radio transceiver (transmitter/receiver), fixed or portable. NOTE: a REP can only operate as a receiver or only as a transmitter.
Radio Fixed Part	RFP	one physical sub-group of a fixed part that contains all the radio end points (one or more) that are connected to a single system of antennas
Receiver Sensitivity		the power level at the receiver input such that the Bit-Error Rate (BER) in the D-field is 0.001
RF carrier (carrier)		the centre frequency occupied by the DECT transmission.
Simplex bearer		a simplex bearer is the MAC layer service that is created using one physical channel. See also duplex bearer and double duplex bearer.
TDMA frame		a time-division multiplex of 10 ms duration containing 24 successive full slots. A TDMA frame start with the first bit period of full slot 0 and ends with the last bit period of full slot 23.
Transmitted Power		mean power delivered over 1 radio frequency cycle
Up link		transmission in the direction of PT to FT

APPENDIX B: COMMON RADIO SYSTEM PARAMETERS

B.1 CIRCUIT NOISE AND NOISE FIGURE

All physical circuits generate noise of some sort. The noise may look like a randomly varying signal and if a very small amplitude signal is to be processed by the circuits, the output may be indistinguishable from the noise produced by the circuit thus limiting the minimum signal level that can be processed by the circuitry. For a radio receiver it is very important that this lower limit on a received signal to be small so that it will be able to recover data from a weak signal and that the transmitted power can be reduced.

There are many different sources of circuit noise. This section outlines some of the more common noise processes and how to analyze their effects in terms of overall system parameters particularly for the Noise Figure (NF).

B.1.1 Noise Processes

There are 3 main types of noise processes that cause the very small random fluctuations in electrical signals. These are Thermal Noise, Shot Noise and Flicker Noise and are caused by different physical interactions at the atomic level.

B.1.1.1 Shot Noise

Shot noise is caused by quantized nature of current. Current is caused by a flow of charged particles (which have a finite lower limit in size equivalent to the charge of an electron) through a boundary. The arrival of these charges are random on the microscopic scale and even though the average flow of charge per unit through this section maybe constant there is actually deviations. This mean squared current variation can be shown using statistical arguments to be independent of frequency with a spectral density of

$$E\{i_n^2(f)\} = 2\,q\,I \qquad [A^2/Hz]. \qquad (B1)$$

In reality this formula breaks down at frequencies with periods much less than the transit time of the carriers across the device (much higher than frequencies that are of concern here).

B.1.1.2 Flicker Noise (1/f)

Flicker or 1/f noise is dependent upon the type of the compound, the process and concentration of defects and its spectral density is inversely proportional to frequency (hence 1/f). This noise is greater in Field-Effect Transistors (FET) than Bipolar transistors because current is conducted close to the surface of the semiconductor in the FETs where the defects are more numerous. At high frequencies shot noise becomes negligible compared to the other white noise sources (shot and thermal) therefore can be ignored but at low frequencies (kilohertz) it must be accounted for.

B.1.1.3 Thermal Noise

Thermal noise was first discovered by J.B. Johnson in 1928. It is caused by the vibrational kinetic energy of a body of charged particles coupling electrically to another device. It was subsequently derived by H. Nyquist using statistical thermodynamics that the thermal noise was related to the generating impedance Z(f) by the relation

$$E\{v_n^2\} = 4\,k\,T\,R(f)\,\Delta f, \qquad [V^2] \qquad (B2)$$

where v_n = thermal noise voltage random variable[V]

$R(f)$ = resistive part of $Z(f)$ [Ω]

T = absolute temperature [K]

k = Boltzmann's constant = $1.38(10^{-23})$ [J/K]

Δf = frequency bandwidth [Hz]

The dependence on the temperature is intuitive as the higher the temperature the more vibration occurs therefore more energy is coupled. For a resistive impedance (R = Z(f)) equation B2 implies that the thermal noise is independent of frequency i.e the spectral density is constant with frequency and the noise can be assumed to be white.

$$S(f) = 4\,k\,T\,R \qquad [V^2/Hz]. \qquad (B3)$$

This in reality would imply that the noise power is infinite if the system is not bandlimited however for the all radio systems the bandwidth of concern is finite (and for DECT very narrow) therefore the noise can be assumed white in that band.

This noise source can be modeled by a mean-squared noise voltage source generator and a resistor (see figure B.1). These noise sources are assumed to be independent and uncorrelated thus for two resistors in series, the expected value of the combined noise generators is

$$E\{(v_1 + v_2)^2\} = E\{v_1^2\} + E\{v_2^2\} + 2\,E\{v_1\,v_2\} = E\{v_1^2\} + E\{v_2^2\} \qquad (B4)$$

therefore the combined noise is

$$E\{v_n^2\} = E\{(v_1 + v_2)^2\} = 4\,k\,T\,(R_1 + R_2)\,\Delta f \qquad (B5)$$

and similarly for two resistors in parallel (use the norton equivalent representation (see figure B.1)

$$E\{v_n^2\} = 4\,k\,T\,(R_1\,R_2 / R_1 + R_2)\,\Delta f. \qquad (B6)$$

Also the maximum available noise power is when the load is matched to the input impedance of the noise source (see figure B.1) and is

$$P_o = E\{v_n^2\} / 4\,R = 4\,k\,T\,R\,\Delta f / 4\,R = k\,T\,\Delta f. \qquad (B7)$$

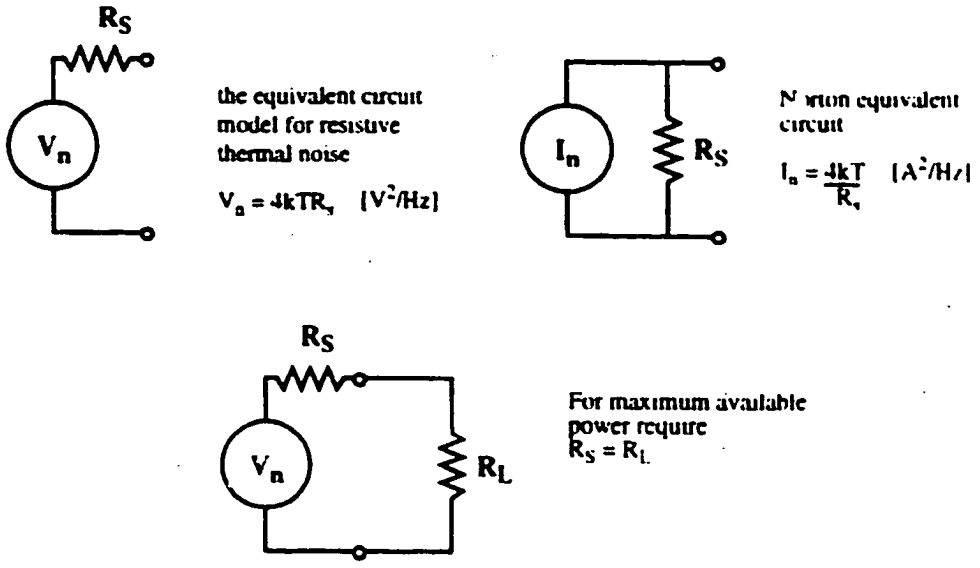


FIGURE B.1 Equivalent Source representation of Resistors and with a noiseless load resistor

This implies that the maximum power available from a resistive noise source is independent of its resistance. This seems counter-intuitive but this is actually consistent with the second law of thermodynamics. If a large resistor is connected to a small resistor at the same temperature, then their is no net power flow from the larger resistance to the smaller one as they are in thermal equilibrium thus the power from the larger resistance must equal the power from the smaller resistance.

B.1.1.4 Noise Figure

There are many ways of quantifying the noise of a system. One way of obtaining a measure of the noise added by a circuit is the noise factor (F) which is defined by the IEEE standards as "The noise factor, at a specified input frequency is defined as the ratio of (1) the total noise power per unit bandwidth available at the output port when the noise temperature of the input is termination is standard (290 K) to (2) that portion of (1) engendered at the input frequency by the input termination."

$$F = \frac{(N_o)_o}{(N_i)_o} = \frac{(N_i)_o + (N_a)_o}{(N_i)_o} \qquad \text{(B8)}$$

where N_o = available output noise power per unit bandwidth referred back to the input.

N_i = available input noise due to source per unit bandwidth referenced to the input.

$(N_i)_o$ = available input noise due to source per unit bandwidth referenced to the output.

N_a = available noise power added per unit bandwidth referred to the input.

NOTE: $()_o$ means referred to output.

In a linear system the output signal is related to the input signal by the gain of the circuit block G e.g $(N_i)_o = G\,N_i$ and $S_o = G\,S_i$

$$F = \frac{GN_i + GN_a}{GN_i} = \frac{N_i + N_a}{N_i} \qquad \text{(B9)}$$

$$\therefore N_a = N_i (F - 1).$$

Also

$$F = \frac{(N_o)_a}{GN_i} \frac{GS_i}{S_o} = \frac{S_i / N_i}{S_o / (N_o)_a}. \qquad \text{(B10)}$$

Therefore

$$F = \frac{\text{Input Signal-to-Noise Ratio}}{\text{Output Signal-to-Noise Ratio}}. \qquad \text{(B11)}$$

Thus the noise factor can be considered as a measure of the decrease of the Signal-to-Noise (SNR) ratio at the output of the network. If N_a is zero (an ideal noiseless network) then the noise factor F = 1. The limitations of the noise factor is that it is limited to networks with at least one input port and one output port, is not useful in determining oscillator or mixer noise contributions and does not take into account the distortion in the signal.

The definition of the Noise Figure (NF) is

$$NF = 10 \cdot \log (F) \qquad \text{[dB]}. \qquad \text{(B12)}$$

Thus an ideal noiseless system with F = 1 will have a noise figure NF = 0 dB.

B.1.1.5 Noise Figure of Cascaded Networks

Suppose there are two 2-port network blocks, block 1 has a gain G_1 and noise factor F_1 and block 2 has gain G_2 and noise factor F_2 that are cascaded together (the input port of block 1 is connected to the input signal, the input port of block 2 is connected to the output port of block1 and the output of the cascaded network is at the output port of block 2). The total

available output power of the overall network is the sum of the noise power at the input port of block 2 (referred to the output), $(N_{i2})_o$ and the noise available from network 2, N_{a2}. Thus the noise factor as defined in (B8) is

$$F = \frac{(N_{i2})_o + (N_{a2})_o}{(N_i)_o}. \tag{B13}$$

Now N_{i1}, the available input noise power per unit bandwidth of block1 is just the overall available input power to the cascaded network, $N_{i1} = N_i$. Therefore referred to the output of the overall network (i.e at output port of block 2), $(N_i)_o = G_1G_2N_i$. Also N_{i2}, the available input noise power per unit bandwidth of block2 referred to the input of block2 is the output noise power from block1, $N_{i2} = G_1(N_{i1} + N_{a1})$ and referred to the output it becomes $(N_{i2})_o = G_2N_{i2} = G_2G_1(N_{i1} + N_{a1})$. Applying all this into (B13) gives

$$\begin{aligned} F &= \frac{G_2G_1N_i + G_2G_1N_{a1} + G_2N_{a2}}{G_2G_1N_i} \\ &= \frac{N_i + N_{a1} + (N_{a2}/G_1)}{N_i}. \end{aligned} \tag{B14}$$

Using (B9) to obtain F_1 and F_2 in terms of N_{a1} and N_{a2} respectively and substituting into (B14) gives

$$F = F_1 + \frac{(F_2 - 1)}{G_1}. \tag{B15}$$

This is the well known expression for noise factor indicating that with a large enough gain in a preceding stage, the overall noise of the system is not severely increased (that is why low-noise amplifiers are always used in the early stages of a receiver chain).Equation (B15) can be used for succeeding stages of a n-stage chain giving the general result

$$F = F_1 + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2} + \ldots + \frac{(F_n - 1)}{G_1 G_2 \ldots G_{n-1}}. \qquad \text{(B16)}$$

B.1.1.6 Sensitivity

The sensitivity of a receiver is the minimum detectable signal. This signal has to be distinguishable from the noise floor of the system by a certain SNR that corresponds to the target performance of a receiver. For digital systems, a common performance measure is the average bit-error rate (BER) and its relation with the SNR of the system can be derived theoretically (with appropriate assumptions) or computed by simulations. Graphs of the BER vs. SNR curves for various modulation schemes can be found in many digital communications text [A3]. With the knowledge of the SNR, the signal strength of the weakest detectable signal can be computed from the following formula

$$P_{min} = SNR \quad (N_i + N_d). \qquad \text{(B17)}$$

Let γ_b be the SNR per bit of the modulation scheme (common theoretical measure of SNR) and R_b be the bit rate. Combining this with (B9) in (B17) gives

$$P_{min} = \gamma_b \cdot R_b \quad N_i \cdot F. \qquad \text{(B18)}$$

Now recall that the available noise power for resistive sources is independent of the resistance (B7) $N_i = kT$ [W/Hz] thus (B18) becomes

$$P_{min} \text{ [dBm]} = 10 \cdot \log(\gamma_b) + 10 \cdot \log(R_b) + NF - 174. \qquad \text{(B19)}$$

B.2 DISTORTION

Most circuits blocks (even those that are designed to be linear) exhibit non-linearities mainly because the transistors used are non-linear devices. The distortion introduced as a results of this can very often disrupt the performance of the system if not accounted for. In this section, the effect of third-order intermodulation is presented and its intercept point

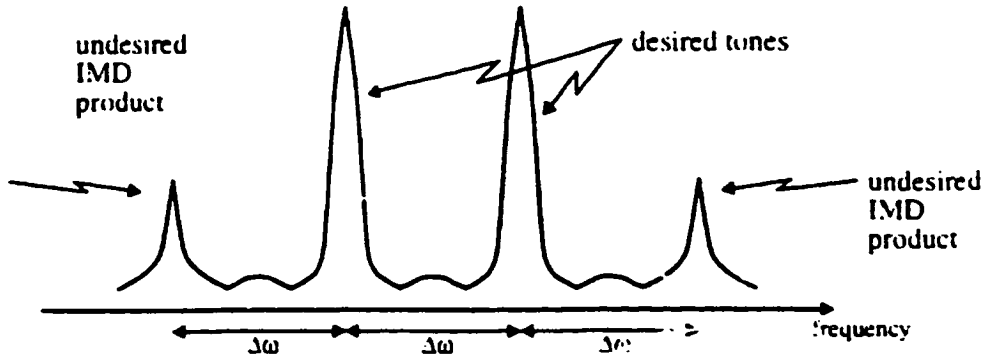


FIGURE B.2 Effects of Intermodulation Distortion on two tones

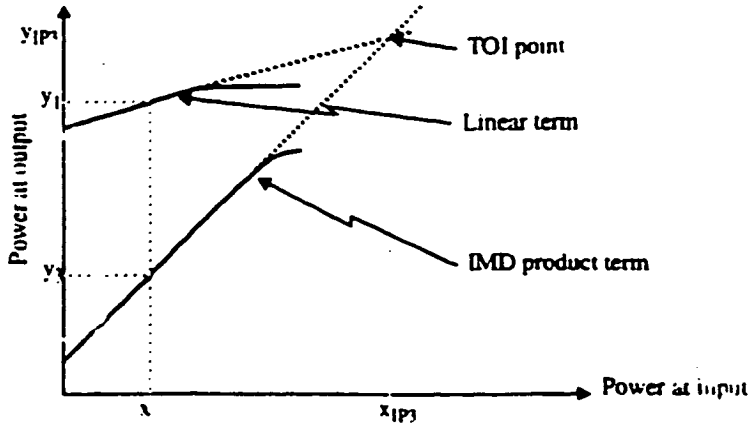


FIGURE B.3 Third order intercept point

shown as a measure of linearity. The calculation of intercept points in cascaded systems is also shown which is required in the linearity analysis of a receiver chain. Another common measure for distortion is the compression point and this is also discussed.

B.2.1 Intermodulation Distortion (IMD)

This is the effect caused by a non-linear transfer function on two tones and is particularly destructive (if ideally a linear transfer function is desired) when the amplitude of the two tones is large. It mainly results in two other tones being produced either side of the desired tones and are called the IMD products (see figure B.2). Thus if the 2 original tones are the RF channels in a multi-carrier radio system then the IMD products will fall in the adjacent RF channels which maybe the actually channel that the receiver is currently tuned to thus causing co-channel interference.

Mathematically the non-linear transfer function can be represented as a power series expansion

$$v_{out} = \sum_{n=0}^{\infty} a_n \left(v_{in}(t)\right)^n \tag{B20}$$

where a_n = the constant coefficients.

Let the input be two tones, $v_{in}(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$ where the difference between ω_1 and ω_2 is much smaller than the $\omega_1 = \omega_2$. The output becomes

$$\begin{aligned} v_{out} = {} & a_0 + a_1 \cdot (A_1\cos\omega_1 t + A_2\cos\omega_2 t) \\ & + a_2 \cdot (A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 \\ & + a_3 \cdot (A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 + \ldots \end{aligned} \tag{B21}$$

The linear term is the desired term and the quadratic term produces undesired tones at the sum and difference of ω_1 and ω_2 which, for a narrowband radio systems, is out of the fre-

quency of interest. The cubic term is the one that produces the intermod products that are located adjacent to ω_1 and ω_2. This can be shown by expanding the cubic term

$$\begin{aligned} a_3 (A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 = {} & a_3 A_1^3\cos^3\omega_1 t \\ & + 3a_3 A_1^2 A_2 (\cos^2\omega_1 t)(\cos\omega_2 t) \\ & + 3a_3 A_1 A_2^2 (\cos\omega_1 t)(\cos^2\omega_2 t) \\ & + a_3 A_2^3\cos^3\omega_2 t. \end{aligned} \tag{B22}$$

The $\cos^3$ terms are again outside the frequency of interest but the other 2 terms will produce tones at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$

$$\begin{aligned} 3a_3 A_1^2 A_2 (\cos^2\omega_1 t)(\cos\omega_2 t) = {} & 1.5 \cdot a_3 A_1^2 A_2\cos\omega_2 t \\ & + 0.75 \cdot a_3 A_1^2 A_2\cos((2\omega_1 - \omega_2)t) \\ & + 0.75 \cdot a_3 A_1^2 A_2\cos((2\omega_1 - \omega_2)t) \end{aligned} \tag{B23}$$

$$\begin{aligned} 3a_3 A_1 A_2^2 (\cos\omega_1 t)(\cos^2\omega_2 t) = {} & 1.5 \cdot a_3 A_1 A_2^2\cos\omega_1 t \\ & + 0.75 \cdot a_3 A_1 A_2^2\cos((2\omega_2 - \omega_1)t) \\ & + 0.75 \cdot a_3 A_1 A_2^2\cos((2\omega_2 - \omega_1)t). \end{aligned} \tag{B24}$$

Thus the IMD product terms are

$$0.75 \cdot a_3 \cdot A_1 A_2^2\cos((2\omega_2 - \omega_1)t). \tag{B25}$$

$$0.75 \cdot a_3 \cdot A_1^2 A_2\cos((2\omega_1 - \omega_2)t). \tag{B26}$$

In most IMD analyses the amplitudes of the 2 tones A_1 and A_2 are equal (to simplify matters). If the amplitude of the IMD products were plotted together with the amplitude of the linear term on a log magnitude scale assuming $A_1 = A_2$, for every increase of 1 dB in the input tone amplitude $A_{1 \text{ or } 2}$ there is a corresponding 3 dB increase in the IMD products (see figure B.3).

B.2.2 Third Order Intercept Point (IP3)

The Third Order Intercept (TOI) point is the intersection of the straight lines extrapolated from graphs of the linear and IMD product terms and can be found using simple geometrical arguments. First the value of x (see figure B.3) is known as that is the input power of a tone. The value y_1 is the output power of one of the desired tones and its ratio with x is just the linear power gain G of the device (the slope of the graph of the linear term is the power gain) and can be easily measured. The value of y_3 is the power of one of the IMD products and can be easily measured using a spectrum analyzer. From these values the output TOI point (OIP3), y_{IP3} can be computed as

$$y_{IP3} = y_1 + \frac{(y_1 - y_3)}{2} \tag{B27}$$

$$\begin{aligned} x_{IP3} &= \frac{1}{G}\left(y_1 + \frac{(y_1 - y_3)}{2}\right) \\ IIP3 &= x_1 + \frac{(x_1 - x_3)}{2} \end{aligned} \tag{B28}$$

where x_{IP3} is the TOI point referred back to the input (IIP3) and $x_1 = y_1 / G$ and $x_3 = y_3 / G$ (i.e. referred back to the input).

NOTE: The measurements of y_1 and y_3 are done when x is low in power so that the device is still relatively linear. As can be seen in figure B.3 at higher power levels the gain deviates from a straight line (it begins to compress) and the actual TOI point is lower than calculated

This intercept point is a measure of the amount of distortion that is created in a receiver and as mentioned before illustrates how well the receiver can resolve a weak signal situated near two interferers. The higher the intercept point the more linear the device. This is because for a larger x_{IP3} the difference between y_1 and y_3 increases for the same input power level x thus the IMD product is less relative to the desired tones.

B.2.2.1 TOI for Cascaded Networks

When two networks are cascaded, the analysis of the distortion created can get rather tedious however in practice assumptions are made to simplify the calculations. First the IMD products generated in the first section is assumed not to produce any other distortion components of relevance in the second stage. The IMD products produced by the second stage is calculated using the equations above assuming that the input to this second stage that will producing IMD products is just the two original tones with the appropriate linear power gain of the first stage (i.e the IMD products and any other distortion components at the output of the first network are ignored).

Thus for equal amplitude tones the resultant output IP3 i.e referred to the output of the overall network as a reference point (OIP3) is given by [A4]

$$OIP3 \approx OIP3_2 - 10 \log\left(1 + \frac{OIP3_2[mW]}{G_2 \cdot OIP3_1[mW]}\right) \quad [dBm] \qquad (B29)$$

where
- OIP3 = output TOI point of cascaded network in dBm.
- $OIP3_2$ = output TOI point of 2nd stage in dBm.
- $OIP3_2[mW]$ = $OIP3_2$ expressed in mW.
- $OIP3_1[mW]$ = output TOI point of 1st stage in mW.
- G_2 = gain of 2nd stage (as a power ratio i.e. NOT in dB).

Another expression for the intercept point but this time referred to the input (IIP3) is

$$IIP3 = IIP3_1 + IIP3_2 - 10 \log\left((G_1 \cdot IIP3_1[mW]) + IIP3_2[mW]\right) \qquad (B30)$$

where
- IIP3 = input TOI point of cascaded network in dBm.
- $IIP3_2$ = input TOI point of 2nd stage in dBm.
- $IIP3_2[mW]$ = $IIP3_2$ expressed in mW.
- $IIP3_1[mW]$ = input TOI point of 1st stage in mW.
- G_1 = gain of 1st stage (as a power ratio i.e. NOT in dB).

Both give the same results.

Note that the linearity of the cascaded network cannot be better than the linearity of the first stage. Intuitively this makes sense as the distortion caused by the first stage is always present in the overall stage (since in most cases the distortions do not cancel out).

B.2.3 Compression Point

When input signals are small most designed to be linear devices behave very close to their specifications and the gain appears constant but as the gain increases the rate of change of the gain decreases. This is called the Gain Compression and one measure is the 1 dB Compression Point (P_{1dB}). This point is defined as that which the power gain is 1 dB below the ideal small-signal gain. This effect can be seen by rewriting (B21) with one a single tone input (i.e. let $A_2 = 0$)

$$\begin{aligned} v_{out} &= a_0 + a_1 A_1 \cos\omega_1 t + a_2 (A_1 \cos\omega_1 t)^2 \\ &\quad + a_3 (A_1 \cos\omega_1 t)^3 + \ldots \\ &= a_0 + a_1 A_1 \cos\omega_1 t + a_2 A_1^2 \frac{(1 + \cos 2\omega_1 t)}{2} \\ &\quad + a_3 A_1^3 \frac{(3\cos\omega_1 t + \cos 3\omega_1 t)}{4} + \ldots \end{aligned} \tag{B31}$$

The amplitude of the tone at freq $\omega_1 = a_1 A_1 + a_3 3(A_1^3)/4$ and for most devices a_3 is normally negative thus the amplitude starts to compress.

APPENDIX C: DERIVING THE COEFFICIENTS OF THE CASCADE-OF-RESONATOR BPΣΔM.

Using the pole and zero of the NTF and STF found in section 4.3.5 and section 4.3.6 the coefficients a_i, b_i and R_j of the cascade-of-resonator structure in figure 4.7 can be computed using the relationships derived in section 4.3.3 and section 4.3.4.

The coefficients R_j are determined by the numerator of the NTF (see section 4.3.3) thus using the zeroes of the NTF the numerator polynomial becomes

$$z^6 + 2.9813z^4 + 2.9813z^2 + 1.$$

And combining these polynomial coefficients with the equations for R_j derived in section 4.3.3 gives the following non-linear simultaneous equations

$$(R_1 + R_2 + R_3) - 6 = 0$$

$$15 - 4(R_1 + R_2 + R_3) + (R_1R_2 + R_1R_3 + R_2R_3) = 2.9813$$

$$R_1R_2R_3 - 20 + 6(R_1 + R_2 + R_3) - 2(R_1R_2 + R_1R_3 + R_2R_3) = 0$$

which reduces to

$$R_1 - R_2 + R_3 = 6$$

$$R_1R_2 + R_1R_3 + R_2R_3 = 11.9813$$

$$R_1R_2R_3 = 7.9626$$

substituting and solving results in the cubic

$$R^3 - 6R^2 + 11.9813R - 7.9626 = 0$$

and solving for the three roots gives

$$R_1 = 2.1366$$

$$R_2 = 2$$

$$R_3 = 1.8634$$

Now using the poles of the NTF found in the optimization process to produce the denominator polynomial coefficients:

$$z^6 + 2.0467z^4 + 1.5056z^2 + 0.3606$$

and then solving for b_j knowing the values of R_j results in:

$b_0 = -0.1323$

$b_1 = -0.0514$

$b_2 = 0.5038$

$b_3 = 0.1277$

$b_4 = -0.9346$

$b_5 = 0.$

Using $R_1 = 2.1366$, $R_2 = 2$, $R_3 = 1.8634$ and that the numerator of the STF is (from the zeroes of the num(STF))

$$z^6 + 0.6056z^4 - 0.6056z^2 - 1$$

combining with the equations for R_j and a_j in section 4.3.4 and solving the linear simultaneous equations for a_j gives

$a_0 = -0.8975$

$a_1 = -0.1530$

$a_2 = 1.447$

$a_3 = 0.3245$

$a_4 = -2.3757$

$a_5 = 0$

$a_6 = 1.$

The coefficients R_j are interchangeable because the numerator polynomial coefficients of the NTF are unchanged if the values of R_j were mixed. This however does result in a new set of coefficients for b_j:

R_1	2.138	2.138	2.0034	2.0034	1.8646	1.8646
R_2	2.0034	1.8646	2.138	1.8646	2.138	2.0034
R_3	1.8646	2.0034	1.8646	2.138	2.0034	2.138
b_0	-0.1223	-0.1323	-0.0983	-0.0983	-0.0295	-0.0295
b_1	-0.0514	-0.0514	0	0	0.0514	0.0514
b_2	0.5038	0.3761	0.5212	0.2658	0.3761	0.2484
b_3	0.1277	0	0.1277	-0.1277	0	-0.1277
b_4	-0.9346	-0.9346	-0.9346	-0.9346	-0.9346	-0.9346
b_5	0	0	0	0	0	0
a_6	1	1	1	1	1	1
a_5	0	0	0	0	0	0
a_4	-2.357	-2.357	-2.357	-2.357	-2.357	-2.357
a_3	0.3245	0	0.3245	-0.3245	0	-0.3245
a_2	1.4447	1.1202	1.4890	0.8400	1.1202	0.1530
a_1	-0.1530	-0.1530			0.1530	0.1530
a_0	-0.8975	-0.8975	-0.7888	-0.7888	0.0295	0.0295
$\max\{a_k, b_i, R_j\}/\min\{a_k, b_i, R_j\}$ excluding b_5	46.2	46.2	24.17	24.17	80.53	80.53

TABLE C1 Coefficients R_j and the corresponding values for a_k, b_k

The values of a_k and b_i corresponding to $R_1 = 2$, $R_2 = 1.8634$, $R_3 = 2$ as it minimized the ratio between the largest value $\max\{a_k, b_i, R_j\}$ and the smallest value $\min\{a_k, b_i, R_j\}$ which is also proportional to the capacitor ratio required in the switched capacitor implementation and thus it is desirable to keep this low.

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